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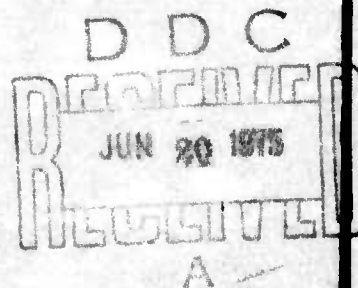| AUTHORITY |
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AFATL-TR-74-208

PILOT'S COCKPIT WEAPON CONTROL PANEL

DELCO ELECTRONICS DIVISION
GENERAL MOTORS CORPORATION
6767 HOLLISTER AVENUE
GOLETA, CALIFORNIA 93017

DECEMBER 1974

DDC

JUN 20 1975

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FINAL REPORT
FOR PERIOD 18 MARCH 1974 - 15 SEPTEMBER 1974

AIR FORCE ARMAMENT LABORATORY

AIR FORCE SYSTEMS COMMAND • UNITED STATES AIR FORCE

EGLIN AIR FORCE BASE, FLORIDA

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20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

A program is described which documents the design, development, fabrication, and test of a Pilot's Cockpit Weapons Control Panel (WCP) together with related support software and processor support equipment. The objective of this program was to develop an integrated, multi-function control/display panel which employs multiple switches whose function and nomenclature can be readily modified under control of a small general-purpose avionics computer.

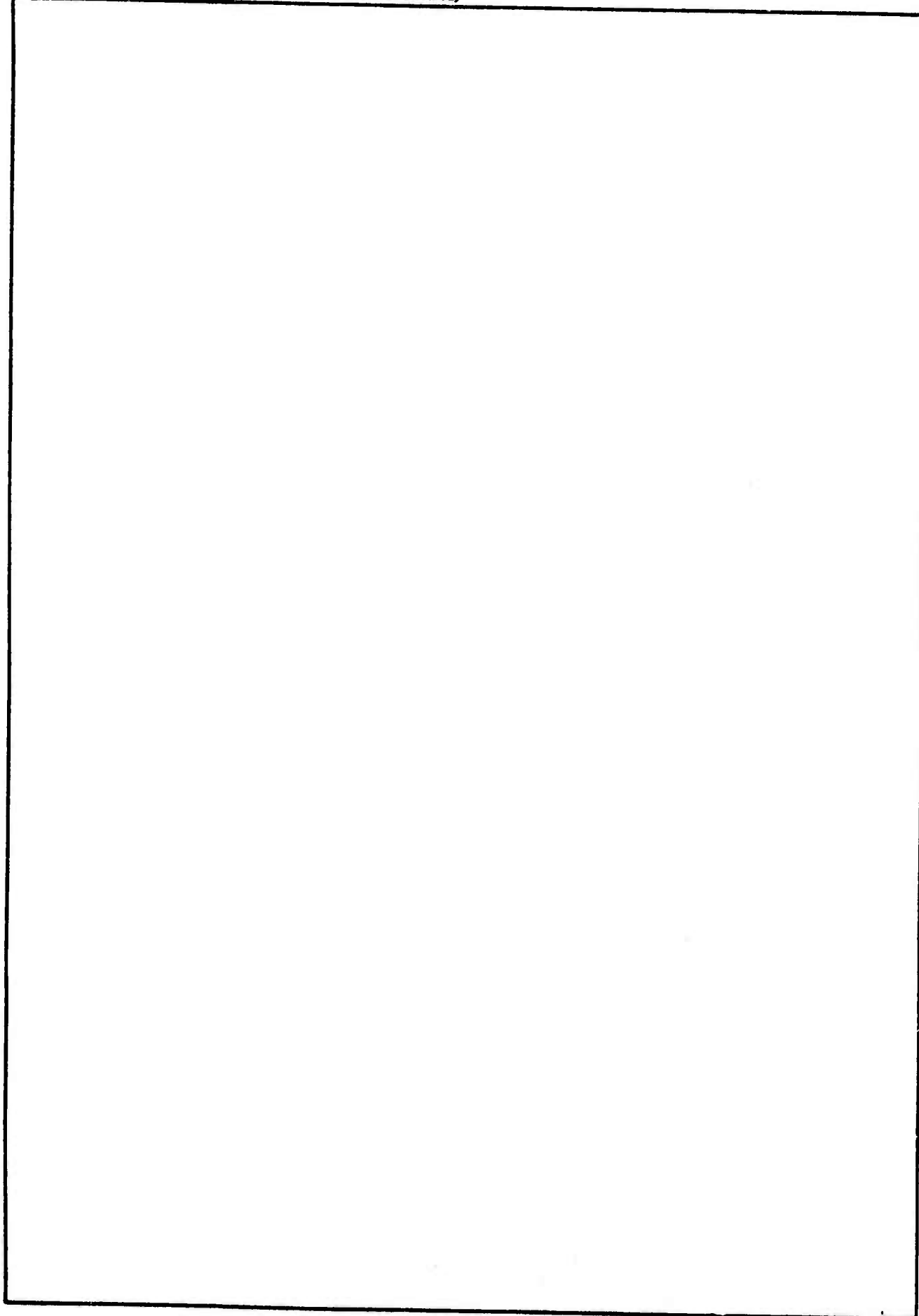DD ,FORM 1473 EDITION OF 1 NOV 65 IS OBSOLETE   UNCLASSIFIED
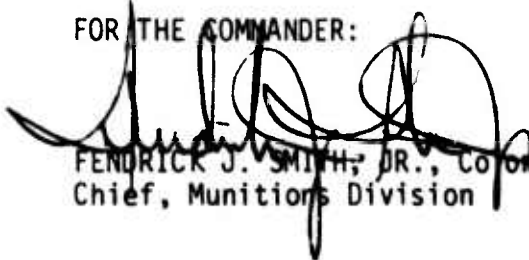
PREFACE

This program was conducted by the Delco Electronics Division of General Motors Corporation, 6767 Hollister Avenue, Goleta, California, 93017 under Contract No. F08635-74-C-0090 with the Air Force Armament Laboratory, Armament Development and Test Center, Eglin Air Force Base, Florida. Captain Glenn M. Rosander (DLJA) managed the program for the Armament Laboratory. This effort was conducted during the period from 18 March 1974 to 15 September 1974.

This technical report has been reviewed and is approved for publication.

FOR THE COMMANDER:

FENDRICK J. SMITH, JR., Colonel, USAF
Chief, Munitions Division

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SECTION I

INTRODUCTION

This report documents the significant items relating to the design, development, fabrication, and test of the Pilot's Cockpit Weapons Control Panel (WCP), related support software, and processor support equipment. Although the majority of the hardware and software designs for this program were extracted from previous developments, their features are so integral to the WCP operation that a discussion of these items is also included for an overall understanding of the system concept and equipment capabilities.

BACKGROUND

The control facet of control and display technology has been unable to keep pace with developments in displays and electronic subsystems because there has been no satisfactory method to change the function of a switch in a way that can be easily recognized and reliably responded to by a human operator. Consequently, while visual presentations have advanced from indicator lights to numerical readouts to multiline alpha-numeric displays and on to fully formatted displays, the control function is still being handled by dedicated switches or by keyboards requiring specially coded data entry.

Meanwhile the operator control task has been expanding. As additional and more sophisticated electronics, including computers, have been added to modern weapon systems, advancing their capabilities, the operator's role has also grown because of the increased option selection available to him. At the same time, control area crowding, particularly in cockpits, is making the operator's task increasingly more taxing because of switch inaccessibility, limited prime viewing area, and non-uniform layouts between like weapon systems.

To solve the problems of restoring the operator's task to a more manageable level, reducing panel space requirements for the control function and taking full advantage of advanced display technology, an integrated, adaptively reconfigurable control and display system is required. Such a system is applicable to numerous military systems including weapon delivery systems. In recognition of the control problem, the Air Force Armament Laboratory, Eglin AFB, Florida initiated the procurement of a Pilot's Cockpit Weapon Control Panel as part of the Aircraft to Weapon Communication Control Program.

The particular problem as viewed by the Eglin AFB personnel is expressed as follows:

> Current aircraft weapons control panels provide only a limited
> control capability. Therefore, aircraft modifications or addi-
> tions are required in order to carry sophisticated weapons.
> The large wire bundles required to connect the control panel
> to the rest of the system are cumbersome and undesireable. The
> objective of this effort is to develop a weapons control panel
> utilizing advanced state-of-the-art techniques which are
> compatible with existing and planned weapons capabilities. This

new control panel will provide control capability throughout the spectrum of weapons and will be interfaced with the host aircraft through a multiplex system.

SCOPE

Under this contract, the following major engineering tasks were performed:

- Design, fabricate, test and deliver a flyable breadboard WCP (prototype).

- Fabricate, test and deliver processor support equipment.

- Design, develop, validate and deliver processor support software.

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SECTION II

TECHNICAL APPROACH

The major objective of this program was to develop an integrated, multi-function control/display panel which employs multiple switches whose nomenclature and function can be legibly and logically modified under control of a small, general purpose avionics computer. The control/display panel is to feature a multi-switch array configured such that the switch functions and nomenclature could be automatically changed in a logical, straightforward manner to reflect only applicable option selections. By implementing such a system, the control aspect of weapon delivery systems will benefit from:

- A significant reduction in the number of switches, displays, and control knobs required, thus reducing prime panel space requirements.

- The need for only one primary control area which could be optimally placed for operator interface, thus increasing systems effectiveness by shortening operator reaction time.

- A simplification of the man-machine interface by presenting only pertinent, logical control options which are viable and relative to the operation in process, thus achieving increased operator proficiency and reduced operator error.

- The ability to add or delete weapon system functions without panel (cockpit) changes, thus greatly reducing modification costs.

Current computer and display technology can be applied to formulate an alphanumeric presentation which portrays an operating system mode and status and which delineates in full word form the selectable options within the mode, as well as exits from the mode. Once a selection has been made and transferred to the computer, software decisions can be made to update the display status and present the next logical set of operator options and/or transfer the selection to the appropriate weapon conditioning and control system. For example, the weapon options could be displayed based upon actual available stores (loaded less expended), with subsequent displays providing options for release/delivery method, fuzing, release quantity, release rate, etc.

A more difficult problem is the integration of the control (switch) functions such that the operator selects the appropriate option in a positive, simple, and reliable manner. From human factors considerations, the ideal solution is for the operator to physically touch the word on the display representing the desired option. This allows his action to be directed to his immediate area of concentration and no translation of the word option to an externally located switch is required. Co-location of the switch with the display also provides the equally important benefit of minimizing panel space requirements.

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To integrate the switch function, the contractor chose to apply a transparent switch matrix design which had been developed to meet this type of requirements. The transparent switch matrix utilizes the electric eye concept of detecting an object by blocking a light beam. A light beam matrix is formed by locating a number of light sources at the top and right side of the display and corresponding receivers along the bottom and left side of the display. When an object is placed in the path of the beams, one or more up-down and right-left beams are blocked, thus locating the object. The matrix is essehtially two-dimensional and can easily be integrated with any type of display.

This means of implementing the switch function offers significant advantages over other methods such as a conductive glass sytem or a cross-wire touch system. These other techniques require physical overlays across the display, are more susceptible to humidity and/or vibration environments, and are inherently less reliable.

The following hardware and software elements were selected to take full advantage of fully developed, available assets:

- A standard Burroughs Corporation Plasma panel, 256-character (8x32) display was selected because of availability and previous airborne applications experience with that type of display.

- The Delco Magic 362 airborne computer was selected as the processor element to simplify interface and software designs.

- The Magic 362 assembler program designed to operate on an Alpha 16 minicomputer centered on-site programming system was selected because of the linkage to a CRT terminal which could be used for display formulation.

- The Magic 362 Computer Control Console was selected as the processor support equipment since it provides the functions required and is a fully developed item.

A system block diagram is shown in Figure 1. Figure 2 is a photograph of the units of the system.
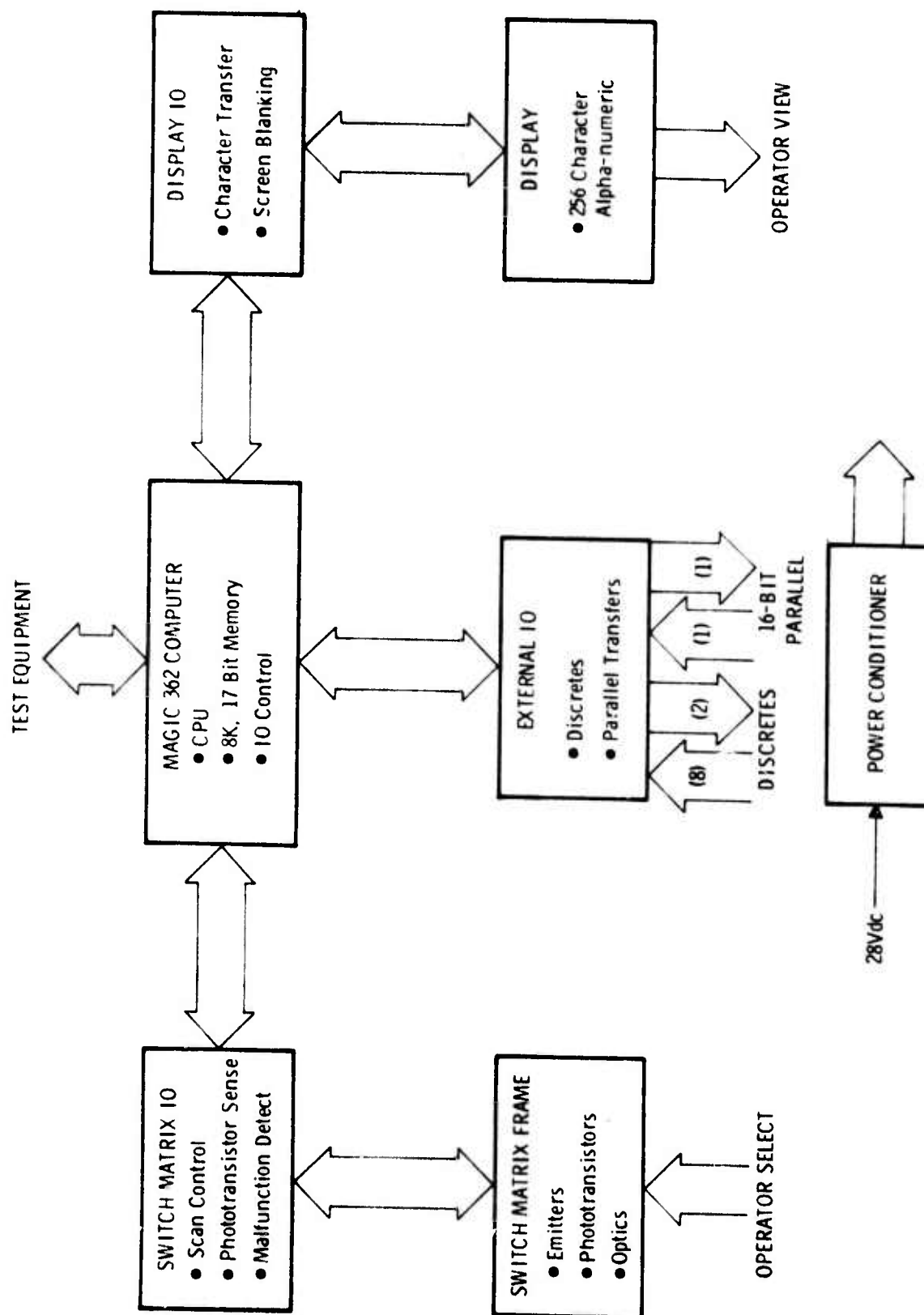
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Figure 1. Weapon Control Panel Block Diagram

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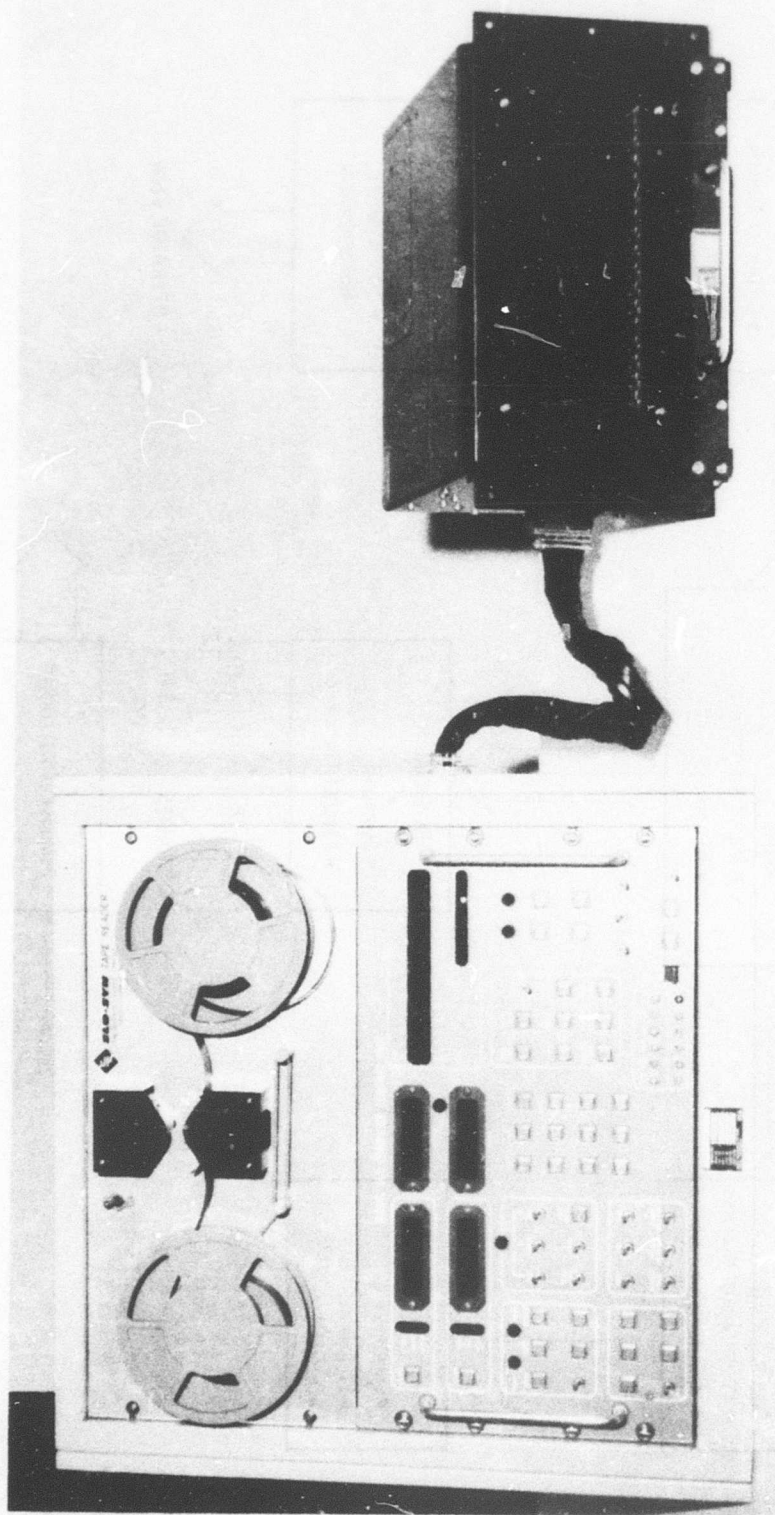
Figure 2. WCP System Units

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SECTION III

HARDWARE IMPLEMENTATION

Switch Matrix

To implement a transparent switch matrix around the light beam interruption principle required tradeoff and analysis to:

- Define the pertinent characteristics required from the light emitters and detectors and characterization of available devices for appropriate selection.

- Design and evaluation of an optical system which can provide the beam focusing necessary to achieve a workable signal-to noise ratio at the receiver, while restricting crosstalk between beams.

- Development of a control/reading technique which, in detecting an object in the switch matrix plane, will be adaptive to object size, discriminate between a valid or non-valid selection, provide switch matrix self-test, and allow the matrix to fail operationally (disable a failed light path with software).

While these tasks were not performed under the auspices of this contract, their results are so significant to the basic theory and operation of the WCP that a summary is included in this report.

The first step in the development of the switch matrix was to survey available emitter and phototransistor devices to select the most likely candidates for this application without entering into a device development. Because infrared emitter spectral response is generally centered in the 900 to 940 - nanometer region and phototransistors typically peak near 900 nanometers, the emitter survey was concentrated in the IR field. The characteristics of 14 IR emitters and 17 phototransistors were compared which resulted in the tentative selection of and test of the Texas Instruments TIL31, Optron OP133, GE SSL35 and Monsanto ME7124 emitters and the Texas Instruments TIL S1 and Optron OP803 and OP805 phototransistors. These device types were tested on a special fixture to obtain comparative performance data with the principal characteristic of interest being the phototransistor output voltage which is the significant system application parameter. The major conclusion derived from this testing was that any of the devices evaluated could be used in the system but that some level of screening and matching would be required. The screening is necessary to ensure reasonable operating margins for the phototransistor threshold between light and no light because of the dispersion in emitter radiation (4:1 measured) and phototransistor response (3:1 measured).

The next major step in the switch matrix design was to design the optical system considering the characteristics of the devices available, background radiation, variations due to temperature, path lengths between emitters and receivers (9.6 inches in the long axis and 3.7 inches in the short axis), display panel reflections, and center-to-center spacing of adjacent light paths (0.28 inch). Using the general criteria of achieving the maximum signal-to-noise ratio and discrimination level at the phototransistor output under high ambient light conditions without imposing exotic mechanical, device, circuit, or optics requirements, a theoretical analysis of the optical system was performed. This analysis concluded, and was generally sub-stantiated by test, that:

- Long axis performance would be marginal without the use of a collimating lens at the emitter end and significant improvement could be obtained in phototransistor output with simple glass plano convex lenses at both ends.

- The use of black walled light tunnels and IR filters at the phototransistor end would provide rejection of ambient light levels above those that would wash out the display itself and thus the use of baffled light tunnels or glare-shields are not required.

- The optoelectric pairs (light beam direction) should be alternated between adjacent positions to reduce crosstalk.

- The alternating of devices and the use of lenses preclude the need to mechanically align the emitter optical axis at assembly.

A complete 8 x 32 switch matrix breadboard was assembled for final validation of the concept and to evaluate detector circuits and control logic options as well as to confirm the calculated operating margins versus influencing para-meters, such as voltage variations, temperature, and variations in emitter/phototransistor characteristics. This breadboard substantiated the validity of the design concept and confirmed that the operating margins were well in excess of circuit variations.

A detailed tradeoff study was conducted to establish the optimum control and readout modes for the panel. This study was particularly important since the basic organization of the switch matrix imposes two significant constraints. First, a true geometric assessment of an object in the switch field cannot be made. At most, the information available is which X and Y axis light beams have been interrupted which transforms into a rectangle regardless of true shape. Second, a switch closure is sensed by the absence of emitter light; thus, a failed emitter or phototransistor appears the same as an object in that path. The pertinent results of this study were:

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- The most efficient switch matrix control from both electronics simplicity and power conservation considerations is provided by sequentially pulsing each emitter and reading the photo-transistor output during the pulse. This provides the capability of 0-Ring the X-axis and Y-axis phototransistors, thus allowing the use of 2 (one per axis) rather than 40 amplifier/detectors and reduces emitter power by a 40:1 factor.

- Little benefit is derived from knowing all of the X and Y light beams that have been interrupted since X-axis interruptions cannot be correlated with Y-axis interruptions, and the computer software is significantly complicated if 40 discretes (switches) must be tested and interpreted.

- Assuming a left-to-right X-axis scan and a top-to-bottom Y-axis scan, where the first interruption in each axis is provided to the computer as an X- and Y-axis position, the data can be used as an X, Y coordinate address which is equivalent to the upper left coordinate of the apparent object rectangle. This can be easily used by the software as an address pointer to determine the switch location.

- By incorporating a double scan, i.e., l-r, t-b, b-t, r-l, the upper left and lower right coordinates of the apparent object rectangle can be provided to the software, thus allowing a reasonableness check to be made on object size, provide means for increased resolution in determining the switch area being activated, and eliminate any sensitivity to a right or left-handed operator.

- In the event of a light path failure, a double scan will produce two values for one axis and no values for the other axis which can be detected as a malfunction.

- Individual software enable/disable control should be provided for each light path to allow exclusion of a failed path from the scan (fail operational) and also to allow reconfiguration of the switch point densities. This latter feature provides increased flexibility for human factors evaluation of the system concept since it allows the exclusion of certain panel areas as active switch areas and also allows reformatting from an 8x32 matrix to such configurations as 8x16, 4x16, 8x8, or 4x8.

- Logic should be provided to reject switch inputs which provide less than two complete sets of coordinates as would occur if the object entered the switch area at any time other than the start of a scan (a normal condition).

1. System Level Operation

The resultant switch matrix design implemented in the WCP reflected the conclusions and results from the analysis and breadboard testing. The

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following provides a description of the switch matrix operation and its operational interface with the processor.

The WCP I/O provides for the recognition and encoding of any of the 256 possible switch matrix switch points where a switch point is spacially located at each of the display character locations. The switch matrix is implemented with 40 IR emitter/receiver pairs configured in 32 columns and 8 rows, thus establishing the 256 unique column/row (X/Y) intersection points. From a functional viewpoint, the operation of the switch matrix is as follows: Each emitter is individually turned on in a fixed sequence and the corresponding receiver is tested for receipt of the light energy. The emitter pulsing sequence starts with column 1 (X01) which is the leftmost column and proceeds through each column in order, ending with column 32 (X32) which is the rightmost column. The pulsing then transfers to the Y or row axis and sequentially goes through the 8 rows starting with row 1 (Y01) which is the top row and ending with row 8 (Y08) which is the bottom row. This X-Y scan is one-half of a switch point read scan. The second half of the read scan pulses the emitters in reverse order, i.e., Y08 through Y01 and X32 through X01. A complete read scan takes 8.2 msec to execute and is repeated continuously until a switch closure is detected.

A switch closure is sensed by the condition of a pulsed emitter and no receipt of light energy by the corresponding receiver. When a switch closure is detected, the row or column number associated with the closure is stored and the emitter pulsing for the remainder of the row or column involved is terminated. If the I/O accumulates an X closure and a Y closure during each half scan of a read scan (4 data points), the scanning routine will be terminated.

If any less than 4 data points are accumulated during a read scan, the data points will be ignored and a new read scan will be initiated (see the discussion on malfunction detection for a special case).

Upon accumulating four data points, the I/O will generate the switch matrix interrupt request. Within the interrupt routine the program should issue the input command to read the switch point data.

Input Command — bits: INP OP CODE | REG CODE | 0 0 1 1 0 1 0
- Read switch closure select
- Display/switch module selection

Input Word — fields: L-R X VALUE | T-B Y VALUE | R-L X VALUE | B-T Y VALUE
- Second half scan data
- First half scan data
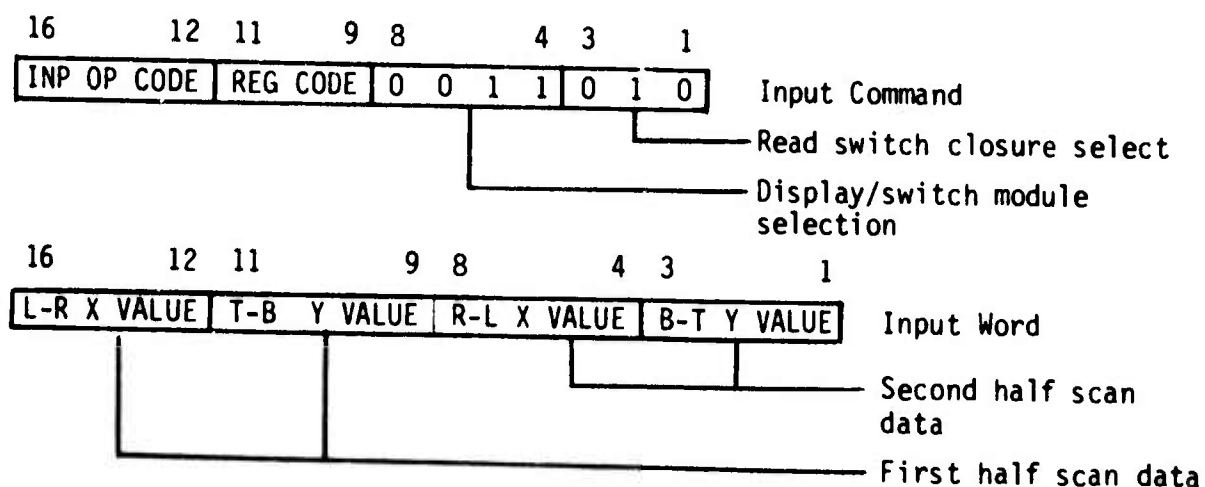
The X and Y values are the binary representation of the detected X and Y switch closures stored during the read scan. The designations (values) are associated with specific emitter/receiver pairs regardless of direction of scan with X01 (leftmost pair) having a value of 00001, X02 having a value of 00010, etc. through X32 (rightmost pair) having a value of 00000; and Y01 (top pair) having a value of 001, Y02 having a value of 010, etc. through Y08 (bottom pair) having a value of 000. This command will not cause an instruction counter skip. Read scans will be resumed after the program has issued the RFI instruction associated with the switch matrix interrupt request.

The switch matrix I/O active switch configuration is controlled by the program by three output commands. These commands provide individual enable/disable control over each of the 40 emitter/receiver pairs which is mechanized such that if any pair is disabled, the receiver output is read as no closure regardless of the actual condition. The program must set the enable/disable state for all 40 emitter/receiver pairs at power turn-on and after recovery from any power transient which caused the WCP to re-initialize and begin instruction execution at location 2000_8 (normal starting address).

```
16        12 11      9  8          4 3      1
OUT OP CODE | REG CODE | 0  0  1  1 | 1  1  0 |          Output Command
                                        |
                                        |————Column 17-32 Enable
                                             select
                              |
                              |————Display/switch module
                                   selection
```

```
16                    1
COLUMN 17-32 |                                 Output Word
   |         |
   |         |————————Column X17 enable
   |              ⋮            ⋮
   |              ⋮            ⋮
   |————————————————————————Column X32 enable
              Enable:  Bit = 1
              Disable: Bit = 0
```

None of the enable commands
will cause an instruction
counter skip.

As part of the WCP built-in test hardware (BITE), the switch logic tests
for a read scan which produces two X closures and no Y closures or two Y
closures and no X closures. Either of these conditions infers an
emitter/receiver pair failure since an inoperative path produces the same
indication as a closed switch. If this condition is detected, scanning
will be terminated, a switch matrix interrupt request will be generated,
and two malfunction discretes will be set. Since either a normal
closure or a switch path failure will produce the same interrupt request,
the program should read the malfunction discretes to determine the
source of the interrupt. These discretes are read by an input command.

```
16        12 11      9  8          4 3      1
INP OP CODE | REG CODE | 0  0  1  1 | 0  1  1 |          Input Command
                                        |
                                        |————Read malf discretes
                                             select
                              |
                              |————Display/switch module
                                   selection
```

```
16 15                                 4  3   2   1
M | 0 0 0 0 0 0 0 0 0 0 0 0 0 | M_S | M_Y | X^M |   Input Word
  |                                    |    |    |
  |                                    |    |    |————X malf discrete
  |                                    |    |        Active:   Bit = 1
  |                                    |    |        Inactive: Bit = 0
  |                                    |    |————Y malf discrete
  |                                    |         Active:   Bit = 1
  |                                    |         Inactive: Bit = 0
  |                                    |————Spare malf discrete
  |————Malf discrete
       Active:   Bit = 1
       Inactive: Bit = 0
```

This command will not cause an instruction counter skip.

The malf discretes are initialized in the inactive state and reset by the RFI instruction associated with the switch matrix interrupt request. To determine which switch path has failed, the program must execute a switch read input command (INP32). The corresponding data word will contain the value of the malfunctioning path in both half-scan data segments and zeroes for the value of the other axis.

2. Functional Operation

The following describes the switch matrix operations including major controls and sequencing. Figure 3 presents the switch matrix electronics in block diagram form.

The computer program issues three output commands to allow enabling/disabling of the individual columns (32) and rows (8) emitter/receiver pair signals. If any pair is disabled by the program, the switch output is read as a no closure regardless of the actual switch condition. The program must set all rows and columns enable state to ON at power turn-on.

The program output discretes are:

      OUT 34 Instruction - Enabling Rows 1 through 8
      OUT 35 Instruction - Enables Columns 1 through 16
      OUT 36 Instruction - Enables Columns 17 through 32

Data is transferred between the computer I/O and the Transparent Switch Electronics (TSE) by means of 16 parallel lines as follows:

      MMI01 through MMI16 - Parallel data word from computer I/O to TSE
      DMI01 through DMI16 - Parallel data word from TSE to computer I/O

The OUT 34 instruction word is decoded by the hardware into the SSD04 discrete which, in turn, allows transfer of data on MMI01 through MMI08 into the Row Enable Storage Register.

The OUT 35 instruction is decoded into the SSD05 discrete which allows the data on MMI01 through MMI16 to be transferred to the Column 1-16 Enable Storage Register.

The OUT 36 instruction is decoded into the SSD06 discrete which allows the data on MMI01 through MMI16 to be transferred to Column 17-32 Enable Storage Register.

DRST* is a discrete initialize pulse (10 μsec). DRST* sets SCAN1 FF to "1" and the Column/Row Up/Down Address Counter to "0".

The counter enable signal, SMINTS="0" and the address counter is ready to count up with receipt of 10 KHz clock, SCLKA, (Count starts after DRST*="1").

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The Column/Row, Up/Down Address Counter counts up generating scan bit times SBT00* through SBT41* in sequence in the Scan X and Y Decoders.

Scanning proceeds in the spatial matrix arrangement from left to right and top to bottom in columns 1 through 32 and rows 1 through 8, respectively. A scan bit time is 100 μsec wide. The output of the decoders are applied to the 32-column and 8-row IR Emitter Drivers. These in turn, one at a time, pulse their respective column and row IR emitters.

At time SBT41*, Scan 1 FF is toggled to "0". (FF change occurs at clock pulse SBT0041B.)

This results in the C/R, U/D Address Counter down count control line being raised to a "1" and the counter now counts down. The Decoder output bit times count down from SBT40* through SBT00*. At bit time SBT00*, the Scan 1 FF output is toggled again to start the address counter to counter up. This cyclic process is continuously repeated until a switch is depressed or a switch malfunction is detected. When the address counter is counting down, the scanning proceeds from Row 8 through 1 and Column 32 through 1 (i.e., B to T, R to L).

The 32 outputs of the column (X) phototransistors (XPDSUM) are wired or together and applied to the X Voltage Comparator. The output of the voltage comparator is a digital signal, XREAD.

Similarly, the 8-row phototransistors wired or output, (YPTSUM), is applied to the Y Voltage Comparator which, in turn, generates the YREAD digital signal.

The XREAD signal, with column enable, COLEN, generates a clocked XLOAD and XDET signals.

The column enable register data is multiplexed with bit times SBT01* through SBT32* to generate column enable signal, COLEN.

The YREAD signal with ROWEN generate a clocked YLOAD and YDET signals. The Row Enable Register data is multiplexed with bit times SBT33* through SBT40* to generate Row Enable signal, ROWEN.

Two consecutive XDET and YDET signals are required to generate a legal switch activation. When this condition is met, a Switch Matrix Interrupt discrete is issued (SMINT/D*).

An XDET* and YDET are ANDed together to generate a YONLY pulse. This, in turn, is used to generate a YMALF12 signal. YMALF12 signifies that only a Y IR beam was detected as interrupted which is not possible during normal switch activation.

Similarly XDET and YDET* signals are used to generate an XMALF12. An XMALF12 means that only an X IR beam was interrupted. XMALF12 and/or YMALF12, when present, usually signify a failure in the emitter driver circuit. The failed position address information is transmitted to the computer I/O as a Switch Malfunction Word after a Switch Matrix Interrupt

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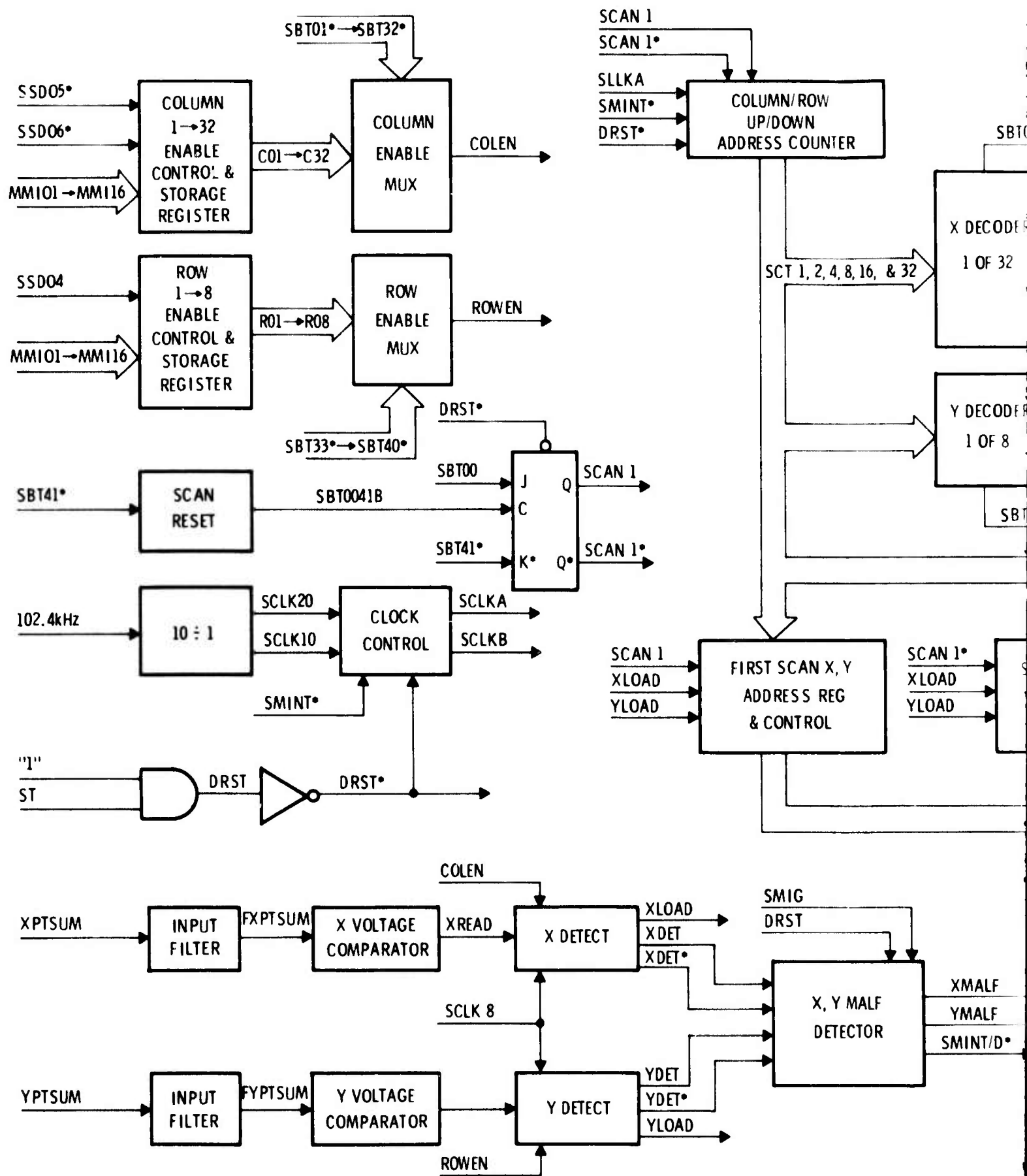
Figure 3. Block Diagram,
Switch Matrix Electronics

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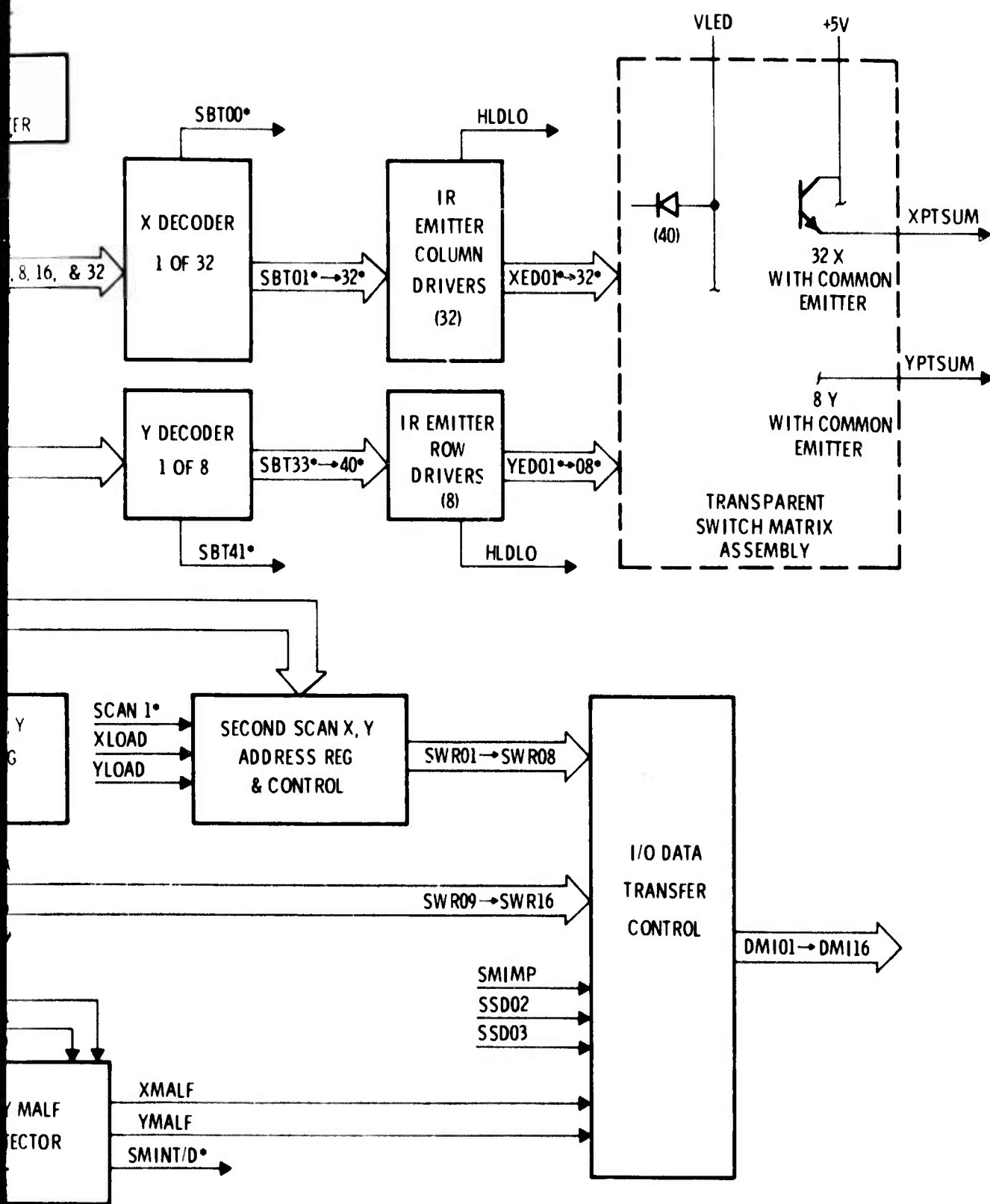signal is generated. The program can then disable the failed position by issuing a revised output discrete word in the proper instruction, i.e., either OUT34, OUT35 or OUT36.

Signals YMALF12* and XMALF12* with signal SMDET4* generate discrete SMINT/D*.

The XLOAD and YLOAD signals are logically combined with Scan 1 and used to clock in the present Column/Row, Up/Down counter address data into the X, Y 1st Scan Address Register. The outputs of this register are parallel signals SWR 09 through SWR 16.

The XLOAD and YLOAD signals with SCAN 1* load the present address information of the Column/Row, Up/Down counter into the X Y 2nd Scan Address Register. The outputs of this register are parallel signals SWR 01 through SWR 08.

These outputs, SWR 01 through SWR 16, are transferred by means of the I/O Data Transfer Control logic to the computer I/O Bus on lines DMI01 through DMI16 when the following occurs:

1. A Switch Matrix Interrupt SMINT is sent from the TSE electronics to the program. The computer receives the SMINT by means of the TRS instruction with an Operand Address 1204_8. An interrupt is generated for either or both:

    a. A malfunction has been detected.
    b. A double scan has been completed with a switch cross point depressed.

2. Once in the SM interrupt routine scanning has been stopped and the SM MALF word should be input, followed by the switch word. This is done by means of the following instruction:

    INP 033 Enable Input SM Malf
    INP 032 Enable Input SM Word

The program must signify completion of the Switch Matrix Interrupt routine by issuing an RFI instruction. When the switch interrupt routine is completed, scanning of the matrix starts over and continues until a switch is depressed or until a malfunction is detected.

3. Physical Description

The switch matrix optical system is contained in a frame as shown in Figure 4. As shown in the photograph, the long axis light paths are staggered. In addition, the light beam direction is alternated between adjacent paths to increase the separation of beams with respect to any given phototransistor. The emitters and phototransistors are
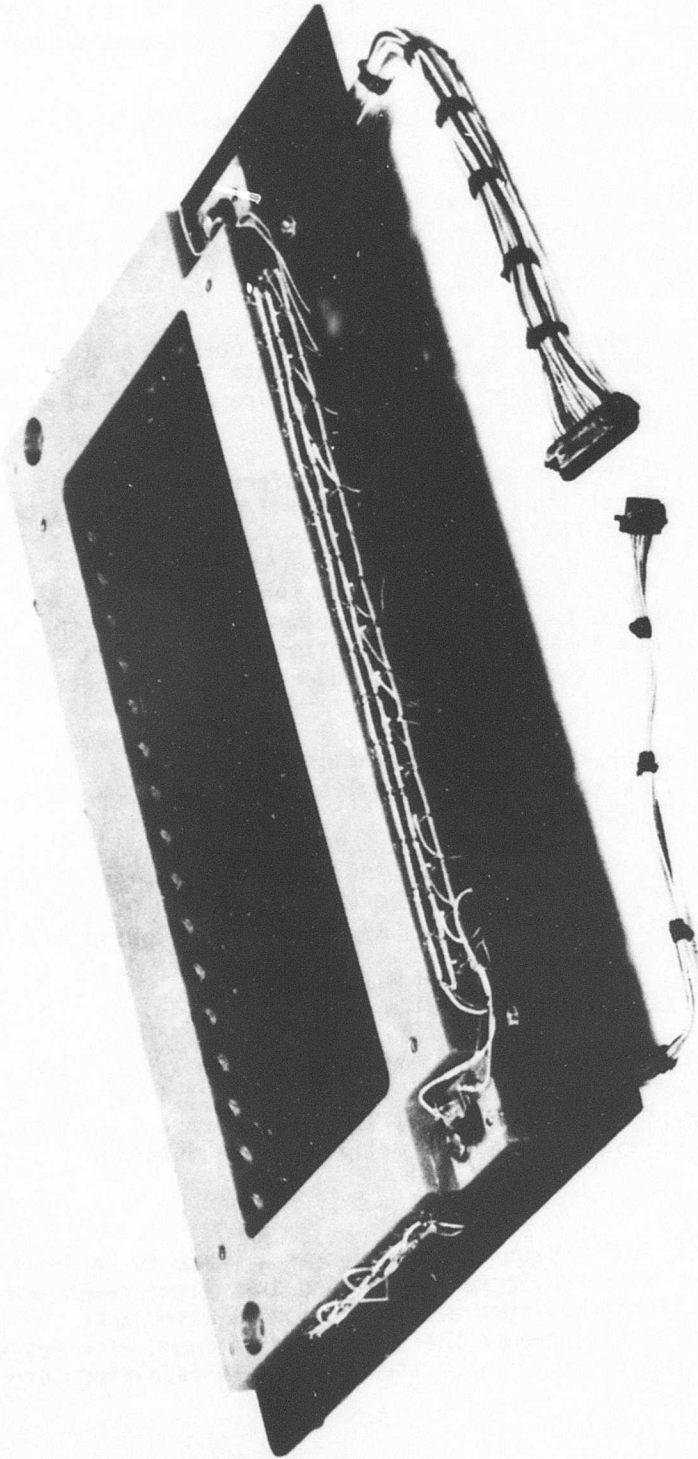
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Figure 4. Switch Matrix Frame

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located on the outer perimeter of the frame, and the lenses are located on the inner surface with the holes through the frame serving as light tunnels.

The frame is permanently attached to the WCP front panel, forming an inseparable assembly. The wiring is connectorized to simplify assembly and enhance maintainability. At the WCP level, the frame, including a contrast enhancement filter, overlays the display, locating a switch point over each of the 256 character locations on the display. As can be seen, this technique is not constrained to a particular display, and the form factor can be adjusted for different beam-to-beam spacing as well as overall frame dimensions. Thus, the frame configuration can be made compatible with any display technology.

Alpha-Numeric Display

The display employed in the WCP is a standard Burroughs Self-Scan® Model BDS40832-200 panel display subsystem which includes a 256-character display, a character generator, a random access memory for self-contained display refresh, drive buffers and demultiplex circuitry, timing and mode control, and anode and cathode drive electronics.

The general characteristics of this subsystem are:

- Character capacity - 256
- Character format - 5x7 dot matrix
- Text format - 32 characters per row, 8 rows
- Dot spacing - 0.04 inch
- Character size - 0.2 inch wide by 0.28 inch high
- Character separation - 0.08 inch between characters
                        0.12 inch between rows
- Brightness - 25 fL nominal
- Contrast ratio - 20:1
- Light spectrum - neon orange
- Panel scan rate - 85 Hz
- Memory access time - 1.75 μsec.

The panel is interfaced to the processor by means of special input/output circuitry. Character data to be displayed is located in 128 words in the program memory with each word containing two six-bit character bytes. The six-bit character codes are a derivation of the ASCII code as shown in Figure 5.

Included in the display I/O is the character generation logic to convert from the modified ASCII codes and the memory and scan logic to maintain the character display. Thus, for any display, the I/O need only be provided one set of 256 6-bit codes.

Two OUT commands are associated with the display I/O, one to clear the display and one to load 256 characters. The clear command is as follows:

B_7 T_S B_4	B_3	B_2	B_1	B_6 B_5: 1 0	1 1	0 0	0 1
0	0	0	0	SP	0	@	P
0	0	0	1	!	1	A	Q
0	0	1	0	"	2	B	R
0	0	1	1	#	3	C	S
0	1	0	0	$	4	D	T
0	1	0	1	%	5	E	U
0	1	1	0	&	6	F	V
0	1	1	1	'	7	G	W
1	0	0	0	(	8	H	X
1	0	0	1	)	9	I	Y
1	0	1	0	*	:	J	Z
1	0	1	1	+	;	K	[
1	1	0	0	,	<	L	~
1	1	0	1	-	=	M	]
1	1	1	0	.	>	N	{
1	1	1	1	/	?	O	}

Figure 5. Modified ASCII Subset for Weapons Control Panel

```
16        12 11       8 7         4 3       1
OUT OP CODE  REG CODE  0  0  1  1  1  1  1        Output Command
                                          └────── Clear display select
                                    └──────────── Display/Switch Module
                                                  Selection
16                                        1
X X X X X X X X X X X X X X X X           Output Word
```
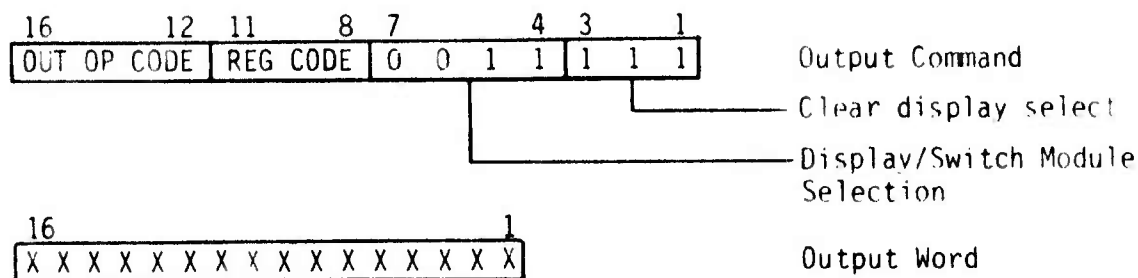
The execution of this command will not cause an instruction counter
skip.

The command to load the display will cause the I/O to extract the
character code data from core memory by means of DMA and update the contents
of the display memory. The DMA access will begin at location 4000_8
and end at location 4177_8, with each memory access providing two
6-bit characters. The $_8$ character locations within each word will be
as follows:

```
16 15 24            9 8 7 6         1
X  X  B6          B1 X X B6        B1    DMA Word
                          └────────────── Even numbered character
               └───────────────────────── Odd numbered character
```
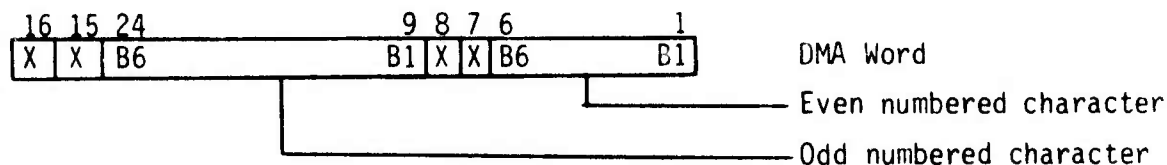
Character data must be stored in memory locations 4000_8 through 4177_8 in
a sequential fashion, i.e., characters 1 and 2 in $_8$ location $_8$
4000_8, characters 3 and 4 in location 4001_8, characters 5 and 6 in
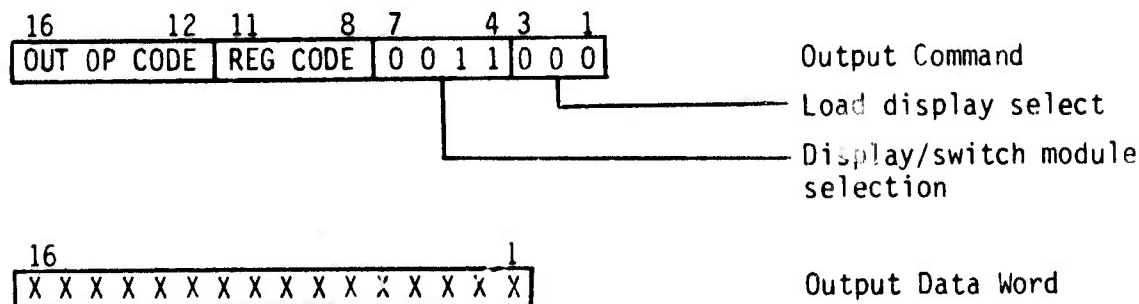$_8$ location 4002_8, etc. Character numbering on the display is
sequential left to $_8$ right and top to bottom starting with 1 and ending
with 256, making the first character number in each row 1, 33, 65, 97,
129, 193, and 225. The output command structure for loading the display
is as shown.

```
16        12 11       8 7     4 3     1
OUT OP CODE  REG CODE  0  0  1  1  0  0  0    Output Command
                                  └─────────── Load display select
                             └──────────────── Display/switch module
                                               selection
16                                        1
X X X X X X X X X X X X X X X X           Output Data Word
```

Once this command is issued, the I/O will proceed through the full 256
characters with the execution time being a function of the display update
rate (approximately 11-3/4 msec for the total display).

If additional load display commands are issued while an update is in process,
the command will be held until the in-process display formatting has been

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completed through all 256 characters. Execution of this command will not cause an instruction counter skip.

Processor

The WCP processor is a Delco Magic 362 general purpose, microprogrammed avionics computer consisting of a central processor, an 8K x 17 bit core memory and an input/output controller. The major features of the processor include:

- Binary, fixed point, two's complement arithmetic with single and double precision operations.

- 2.9 μsec Add/Subtract/Load execution time

- 16 program accessible registers

- 1.4 μsec memory cycle time

- Memory parity

The processor instruction repertoire and execution times are given in Figure 6.

External I/O

In addition to the switch matrix and display I/O, the WCP provides interfaces to external systems. Included are eight 28 VDC input discretes, two 28 VDC output discretes, a 16-bit parallel channel to another computer, and a 16-bit parallel channel from the other computer. The specific requirements for the external I/O were modified during the contract with the final configuration described below.

1. External Input Discretes

The WCP I/O wll accept up to eight 28 Vdc discretes. The discretes are input through optically coupled isolaters which are referenced individually to a discrete return signal. The input discrete channel is mechanized to generate an interrupt request when any of the eight inputs changes state from either a high to a low or from a low to a high.

    A. Signal Interface Characteristics

1.	Type:	Double-ended
2.	Voltage:	Logic "1"=16+6 Vdc
		Logic "0"= open circuit or 0+.9 Vdc
3.	Load Resistance:	3.9 Kohms + 5%
4.	Transients:	Up to 80V per MIL-STD-704A

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MNEMONIC	DESCRIPTION	COMPUTER CLOCKS	EXECUTION TIME (µsec)
	ARITHMETIC		
ADD	Add memory to A register, result in A	12	2.930
ADM	Add A register to memory, result in memory	18	4.395
ARR	Add register to register	7	1.709
ADP	Add double word in memory to A and B registers	18	4.395
DIV	Divide A and B registers by memory, quotient in A	48	11.719
IRI	Increment register by operand address	6	1.465
MDP	Multiply A and B registers by double word in memory, result in A, B, X, and Y registers	141	34.424
MPY	Multiply A register by memory, result in A and B	30	7.324
MSK	Mask A register with memory, result in A	12	2.930
SDP	Subtract double word in memory from A and B	18	4.395
SRR	Subtract register from register	7	1.709
SUB	Subtract memory from A register, result in A	12	2.930
TCC	Test sign of first register and carry to second register	10	2.441

Figure 6. WCP Instruction Repertoire

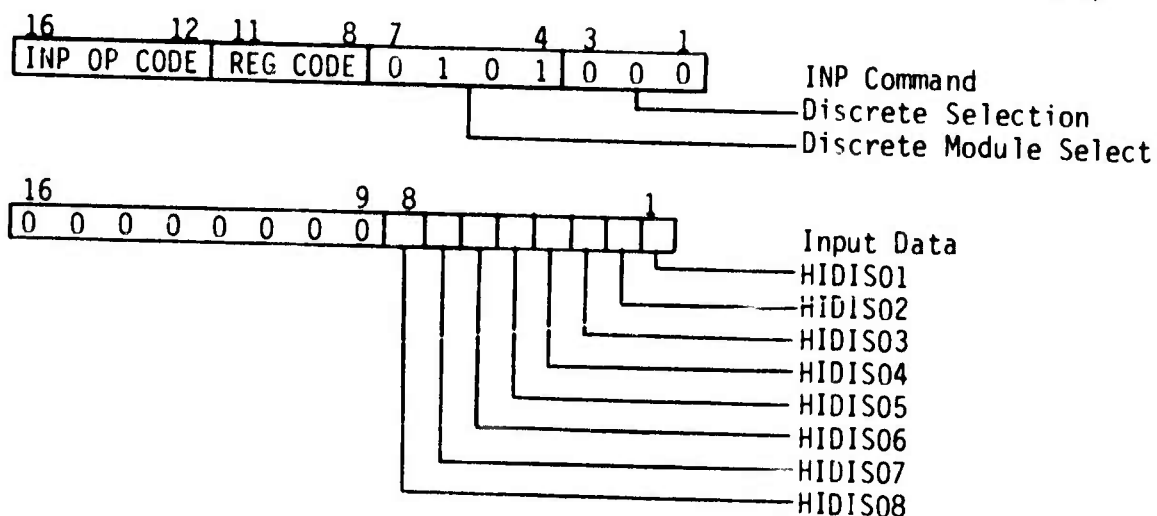| MNEMONIC	DESCRIPTION	COMPUTER CLOCKS	EXECUTION TIME (μsec)
	SHIFT		
RTE	Rotate combined A and B registers	11	2.686 + 0.244N
SFA	Shift A register	9	2.197 + 0.244N
SFB	Shift B register	9	2.197 + 0.244N
SFD	Shift double word in A and B registers	12	2.930 + 0.244N
SFX	Shift X register	10	2.441 + 0.244N
SFY	Shift Y register	10	2.441 + 0.244N
	LOAD/STORE		
LDA	Load A register from memory	12	2.930
LDD	Load A and B registers from double word in memory	18	4.395
LRI	Load register with operand address	6	1.465
LRM	Load register from memory	12	2.930
LRR	Load register from register	7	1.709
SRM	Store register in memory	12	2.930
STA	Store A register in memory	12	2.930
STD	Store A and B registers in memory (Direct)	18	4.395
STD	Store A and B registers in memory (Relative)	19	4.639
Z	Zero register	7	1.709

Figure 6. WCP Instruction Repertoire
(continued)

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MNEMONIC	DESCRIPTION	COMPUTER CLOCKS	EXECUTION TIME (μsec)
	BIT ACCESS		
RB	Reset selected bit in memory	18	4.395
SB	Select bit in memory	18	4.395
SNS	Skip if selected bit not set	12	2.930
	CONTROL		
JMP	Jump unconditionally	7	1.709
JOM	Jump if register minus	7	1.709
JOP	Jump if register positive	7	1.709
JOZ	Jump if register zero	7	1.709
RFI	Return from interrupt	13 + IOW	3.174+IOW
RFS	Return from subroutine	14	3.418
SRG	Skip if register greater than memory	12	2.930
TRA	Transfer unconditionally (indirect)	12	2.930
TRS	Transfer to subroutine (indirect)	13	4.395
	INPUT/OUTPUT		
INP	Input to register	6 + IOR	1.465+IOR
OUT	Output from register	6 + IOW	1.465+IOW

IOR = I/O read time (minimum 0.732 microseconds)
IOW = I/O write time (minimum 0.732 microseconds)
N   = Number of bits shifted

Figure 6. WCP Instruction Repertoire
(concluded)

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B. Programming Interface Characteristics

Input discretes HIDIS01 through HIDIS08 shall be available to the program from the Discrete Module. Program access shall be with an INP command whose particulars shall be as indicated below. The INP command shall not cause an instruction counter skip.


```
 16        12 11      8 7         4 3       1
[INP OP CODE| REG CODE| 0  1  0  1 | 0  0  0 ]    INP Command
                                              Discrete Selection
                                              Discrete Module Select
```

```
 16                      9 8           1
[0  0  0  0  0  0  0  0 |  |  |  |  |  |  |  | ]   Input Data
                                              HIDIS01
                                              HIDIS02
                                              HIDIS03
                                              HIDIS04
                                              HIDIS05
                                              HIDIS06
                                              HIDIS07
                                              HIDIS08
```

The sense of the input data is true, i.e., a logic "1" input will be represented as a one and a logic "0" input will be represented as a zero.
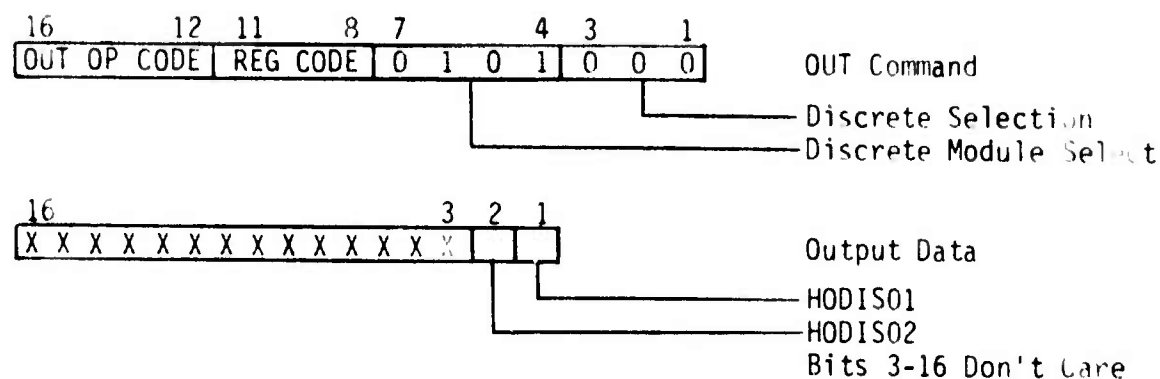
2. External Output Discretes

The WCP I/O will output two 28 Vdc discretes through optically coupled isolators. These outputs shall be powered individually from external 28 Vdc discrete voltages and referenced to individual discrete lows.

A. Signal Interface Characteristics

1. Type: Three-wire, with power externally connected to the high and the load connected from the output to an externally supplied ground.

2. Power: External 28 Vdc+6 Vdc with transients to 80V per MIL-STD-704A, 100 mamps.

3. Source Impedance: Logic "1": Discrete power less transistor drop
                      Logic "0": 20K to ground

B. Programming Interface Characteristics

Output discretes HODIS01 and HODIS01 shall be controlled by the program by an OUT command to the Discrete Module. Issuance of the OUT command shall not cause an instruction counter skip.

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```
 16        12  11     8  7        4  3     1
|OUT OP CODE| REG CODE| 0  1  0  1| 0  0  0|     OUT Command
                            |                └─── Discrete Selection
                            └──────────────────── Discrete Module Select

 16                           3  2  1
|X X X X X X X X X X X X X X| |  |  |           Output Data
                             |     └──────────── HODISO1
                             └────────────────── HODISO2
                                                 Bits 3-16 Don't Care
```

The sense of the output data is such that the discrete is in the high (active) state when the output data bit is a one.

3. Parallel Input Channel

The WCP I/O provides the program with an input communications from a ROLM 1602 Parallel I/O Buffer 3540 output channel. The channel consists of a 16-bit parallel information path to the WCP, a control path to the WCP, and a control path from the WCP. Control of the channel is exercised by the WCP program and by the Rolm 1602; thus, the word rates are variable.

A.   Signal Interface Characteristics

The following signals comprise the Parallel Input communications channel.

Signal	Source	Definition
DO'N' where 'N' = 0 through 15	ROLM 1602	Input data paths where DO 0 is the least significant bit of the transfer
OUT BUSY*	ROLM 1602	Control path to WCP
EXT GATE	WCP	Control path to Rolm 1602

This interface shall exhibit the following characteristics:

1. Type: Single-ended TTL
2. Source: Open collector TTL element with standard drive capability (SN5403, SN5405, or equivalent)
3. Load - WCP: 1K ohms to V_{CC} and one standard TTL element.
4. Load-1602:   330 ohms to V_{CC}, 390 ohms to ground and one standard TTL element.
5. Sense: The data paths shall be true signals, i.e., a high shall represent a logic "1". The 1602 control path shall be a false signal (a low signifies data available on the data paths) and the WCP control path shall be a true signal (a positive pulse signifies that the WCP has read the data).
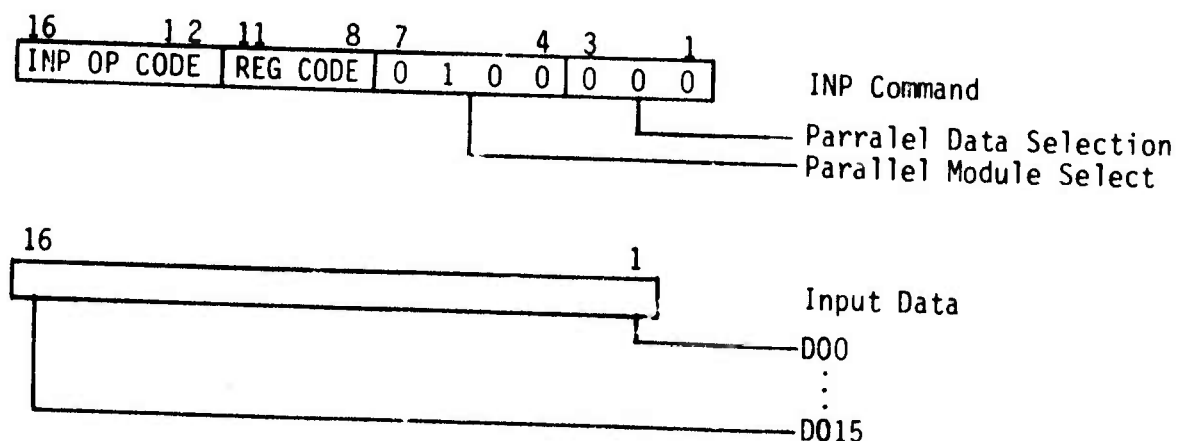
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This interface is based upon the 3540 being wired to always enable the output data lines and to have OUT DONE set by the WCP.

In operation, OUT BUSY* will normally be in the high (no data) state and EXT GATE will be in the low state. To initiate a transfer, the 1602 shall drop OUT BUSY* to signify that a transfer is to be made and place the information on data lines D00 through D015. Upon sensing the fall of OUT BUSY*, the WCP will signal the program by generating an interrupt request. During the interrupt routine, the program will execute the INP command assigned to read the parallel channel. The RFI instruction used to terminate the routine will be sensed by the WCP I/O as a command to pulse the EXT GATE line. The fall of the EXT GATE pulse will cause the 1602 to raise the OUT BUSY* line and to reset OUT DONE in the 1602, thus clearing the channel to allow another transmission.

The 1602 program must account for a unique case which is related to WCP signals in the event of a power interruption which would cause loss of the logic power in the WCP. The signal EXT GATE is normally low and is pulled up in the 1602. If logic control is lost in the WCP because of power loss, the 1602 circuitry will sense a high on this signal due to the pull up network and when power is restored the signal will be returned to the low state. Under these conditions the 1602 would sense a completion of a transmission when none was intended. It should be noted that this would only be a problem if a transmission request had been made by the 1602 and the interruption occurred before the transmission was completed and if the source of the interruption did not affect the 1602 or if a transmission was requested while the WCP was not powered or was in the process of being powered-up.

B.   Programming Interface Characteristics

The parallel input data is read with an INP command which should only be executed during the parallel input data interrupt subroutine. To signify that the data processed to the program is valid, the I/O shall force an instruciton counter skip for OUT BUSY (data valid) and not force a skip if the INP command is executed when the input data is not valid. The parallel input interrupt subroutine should be minimized to maximize the transfer rate to the computer in that new data will not be presented until the RFI associated with the subroutine has been issued.

16	12	11	8	7		4	3		1	
INP OP CODE		REG CODE		0	1 0 0		0	0 0		INP Command

Parralel Data Selection
Parallel Module Select

16		1	
			Input Data

D00
:
D015

28

4. Parallel Output Channel

The WCP I/O provides the program with an output communications channel to a Rolm 1602 Parallel I/O Buffer 3540 input channel. The channel consists of a 16-bit parallel information path from the WCP, a control path from the WCP and a control path from the 1602. Control of the channel is exercised by the WCP program and by the 1602, thus word rates are variable

A.   Signal Interface Characteristics

The following signals comprise the Parallel Output communications

Signal	Source	Description
DI'N' where 'N'=0 through 15	WCP	Output data paths where DIO is the least significant bit of the transfer
IN CLK	WCP	Control path to 1602
IN BUSY*	1602	Control path to WCP

This interface shall exhibit the following characteristics:

1. Type: Single-ended TTL
2. Source: Open collector TTL element with standard drive
                   capability (SN5403, SN5405, or equivalent)
3. Load-WCP: 1K ohm to V_{CC} and one standard TTL element
4. Load-1602:   330 ohms to V_{CC}, 390 ohms to ground and one
                   standard TTL element.
5. Sense: The data paths shall be true signals, i.e., a
                   high shall represent a logic "1". The 1602
                   control path shall be a false signal (a low
                   signifies that the 1602 is ready to receive
                   data) and the WCP control path shall be a true
                   signal (a positive pulse loads the data into
                   the 1602 register).

A transition of the IN BUSY* signal to the low state will cause the WCP I/O to generate a parallel output interrupt request which will be reset by the associated RFI instruction.   IN BUSY* being low signifies that the communications channel is open. The WCP parallel output OUT command will result in the associated data being placed on the DI lines and the generation of a pulse on the IN CLK line. The fall of IN CLK will cause the 1602 to store the data word in an I/O register, raise the IN BUSY* line and reset the IN DONE signal (internal to the 1602).

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The same unique case described for the EXT GATE signal for the input channel applies to the IN CLK signal for the output channel.

B.   Programming Interface Characteristics

The way in which this channel operates will be highly dependent upon both WCP and 1602 programming. Primary control of the channel is governed by the IN BUSY* signal which must be in the low state when a transfer is made. IN BUSY* is dropped as a result of a 1602 command, and the transition from the high to the low state is sensed by the WCP I/O which, in turn, results in the generation of a parallel output interrupt request in the WCP I/O. The IN CLK signal is used to cause the 1602 to store the information on the 16 data lines in an I/O register, raise IN BUSY*, and reset the internal IN DONE signal. At this point the channel is disabled from further transmissions until the 1602 reads the previous transmission and again drops IN BUSY*. IN CLK is a 1 µsec (nominal) pulse which is generated as a result of the WCP OUT40 command after the data word is available on the DI lines.

This mechanization of the channel control allows the 1602 to keep the channel open at all times except for short periods immediately following a transfer, thus accommodating WCP originated transfers as well as responses to 1602 requests. In the operational configuration, the WCP software will have to keep track of the status of the channel since the interrupt request will not necessarily signify that a transfer is to be made but rather that the channel is open. It will be necessary that the WCP interrupt routine associated with the parallel output interrupt not execute an OUT40 since it would be possible for the 1602 to read the transfer and reopen the channel prior to the associated RFI instruction clearing the WCP interrupt request. Were this to happen, the WCP would have failed to sense the fall of IN BUSY* and thus be unaware that another transfer could be made result- ing in a permanent hangup of the channel.

An open channel is signified by the parallel output interrupt request and the parallel output data is sent to the I/O with an OUT command. The I/O will force an instruction counter skip if IN BUSY* is low (1602 ready to accept data) when the OUT is issued. If the OUT command is issued when IN BUSY* is high (channel busy) the I/O will not force an instruction counter skip.

Out Command

Parallel Data Selection
Parallel Module Select

Output Data

DI0
.
.
DI15

30
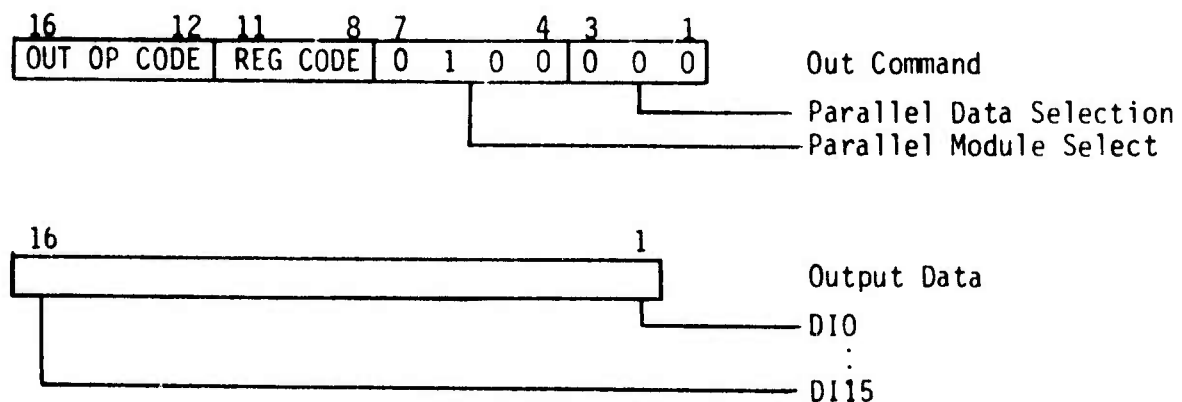
Interrupts

The WCP I/O uses an instruction insert technique to implement interrupts
with the inserted instruction being a TRS. Each interrupt source will
reset a TRS with a specific address, and the program must signify the
completion of the interrupt routine by issuing an RFI instruction, again
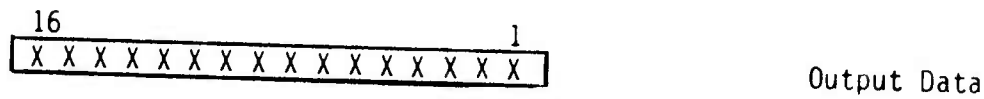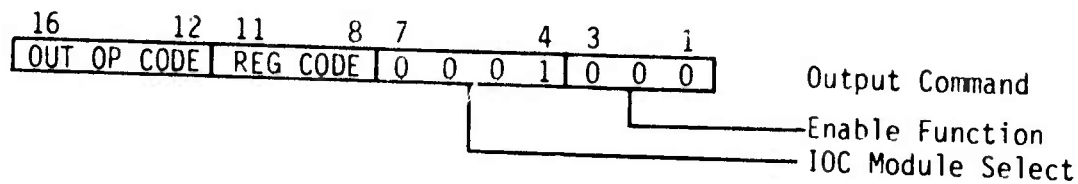with the address associated with the interrupt being processed.

The interrupts are hardware organized in a specific priority structure
which accommodates six instruction insert requests: five associated with
I/O and one associated with the test equipment. The test equipment
interrupt is a unique case in that any instruction may be inserted and no
RFI is involved   The functioning of the priority string is such that (a)
if more than one request occurs, the request with the highest priority will
be serviced first; (b) if a higher priority request occurs during the
execution of a lower priority routine, the higher priority request will be
granted and interrupt the routine in process; and (c) if a lower priority
request occurs during the execution of a higher priority routine, the
lower priority request will be held until the routine in process is
completed. The priorities, TRS addresses, and RFI addresses for the
interrupt requests are as follows:

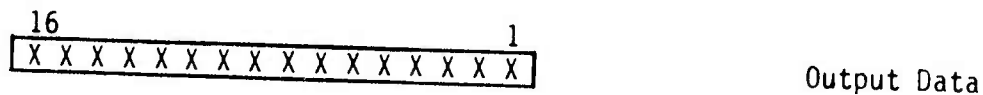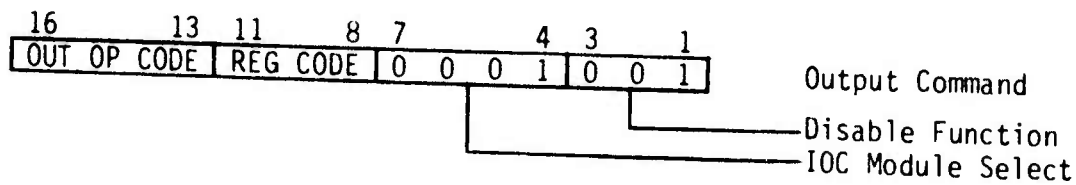| Priority	Function	TRS Address	RFI Address
1	Input Discretes	1206	06
2	Parallel Input Channel	1205	05
3	Switch Matrix	1204	04
4	Parallel Output Channel	1202	02
5	Real Time	1203	03
6	Test Equipment	N/A	N/A

With the exception of the Input Discrete interrupt, the WCP I/O will
establish an insert request based upon the interrupt condition and reset
the request as a result of the RFI instruction. Any same priority inter-
rupt conditions which occur subsequent to establishing the insert
request but prior to the associated RFI will be ignored. The Input Dis-
crete interrupt is a unique case where the insert request will be based
upon the interrupt condition but will be reset by an INP50 (Read Input
Discretes) instruction, thus allowing another interrupt condition to be
stored prior to completion of the Input Discrete Interrupt Routine. This
does require that the programmer include one INP50 in this interrupt
routine.

The program has control over enabling or disabling all WCP I/O interrupts
but not the test equipment interrupt. This control is implemented with
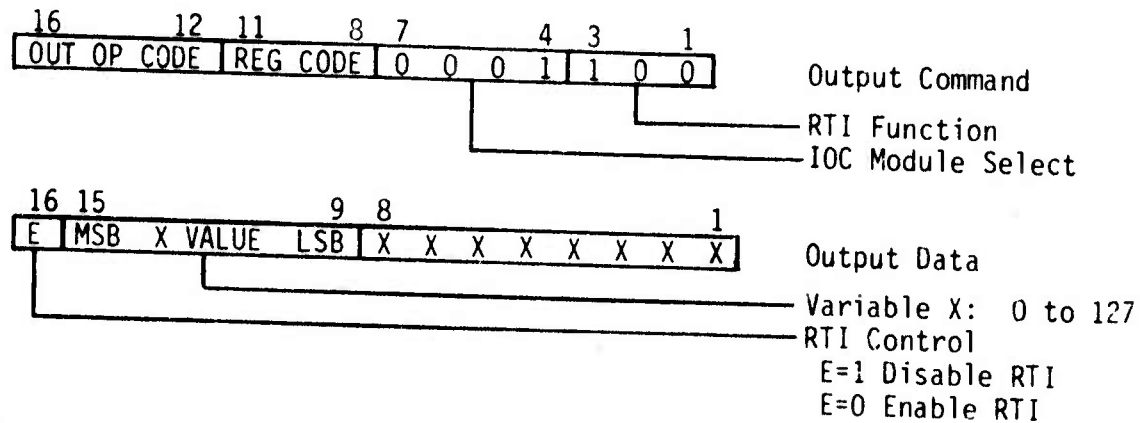OUT commands as follows:

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Interrupt Enable

```
 16        12 11       8 7           4 3       1
| OUT OP CODE | REG CODE | 0  0  0  1 | 0  0  0 |      Output Command
                                   |_____Enable Function
                              |_____IOC Module Select
```

```
 16                                            1
| X X X X X X X X X X X X X X X X |                    Output Data
```

Interrupt Disable

```
 16        13 11       8 7           4 3       1
| OUT OP CODE | REG CODE | 0  0  0  1 | 0  0  1 |      Output Command
                                   |_____Disable Function
                              |_____IOC Module Select
```

```
 16                                            1
| X X X X X X X X X X X X X X X X |                    Output Data
```

All I/O interrupts are disabled by hardware initialization circuitry at power turn-on.

A real-time interrupt signal is generated by the WCP I/O, the frequency of which is determined by the program. This interrupt must be individually enabled by the program and can be individually disabled. The program control of the RTI is an OUT command as follows:

```
 16        12 11       8 7           4 3       1
| OUT OP CODE | REG CODE | 0  0  0  1 | 1  0  0 |      Output Command
                                   |_____RTI Function
                              |_____IOC Module Select
```

```
 16 15              9 8                         1
| E | MSB  X VALUE  LSB | X  X  X  X  X  X  X  X |     Output Data
                   |_____Variable X:  0 to 127
             |_____RTI Control
                                                          E=1 Disable RTI
                                                          E=0 Enable RTI
```
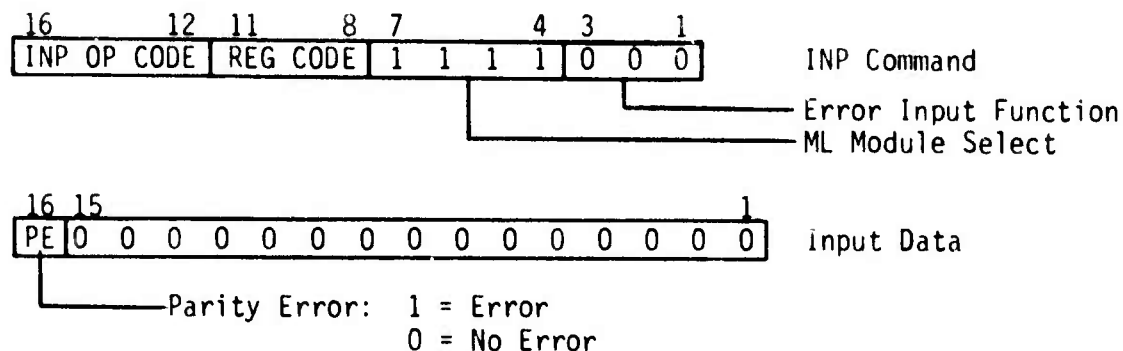
The frequency of the RTI is given by

$$f = \frac{2000}{X+1} \text{ Hz}$$

where X is the program variable giving the RTI a frequency range of 2000 Hz (0.5-msec interval) to 15.625 Hz (64-msec interval).
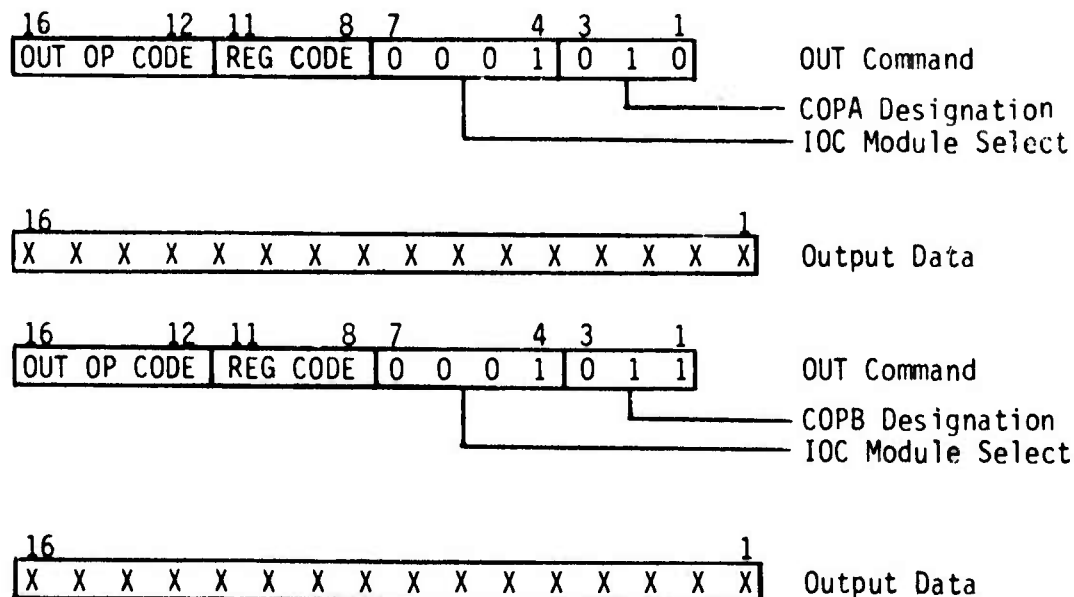
Built-in Test

In addition to the switch matrix malfunction detection circuitry, the WCP provides BITE for memory parity and for a check on the software running time. The WCP I/O generates two internal error flag discretes which are available to the program: one from the Memory Logic Module and one from the IOC Module. These discretes, PARE and COPE, are read with INP commands and signify a memory parity error and too long a program cycle time, respectively.

PARE. The parity error flag is read with an INP command, the execution of which does not cause an instruction counter skip. Execution of the INP command will cause the error latch to be reset.

```
 16        12  11       8  7         4  3       1
| INP OP CODE | REG CODE | 1  1  1  1 | 0  0  0 |   INP Command
                                          |_____ Error Input Function
                            |_____ ML Module Select
```

```
 16 15                                          1
| PE | 0  0  0  0  0  0  0  0  0  0  0  0  0  0  0 |   Input Data
  |_____ Parity Error:  1 = Error
                               0 = No Error
```

COPE. The IOC Module provides a time check on the operational program based upon the sequential issuance of OUT commands within a specified time frame. The time between OUT commands shall not exceed 120 msec or a COP Error will be latched. The OUT commands do not cause an instruction counter skip.
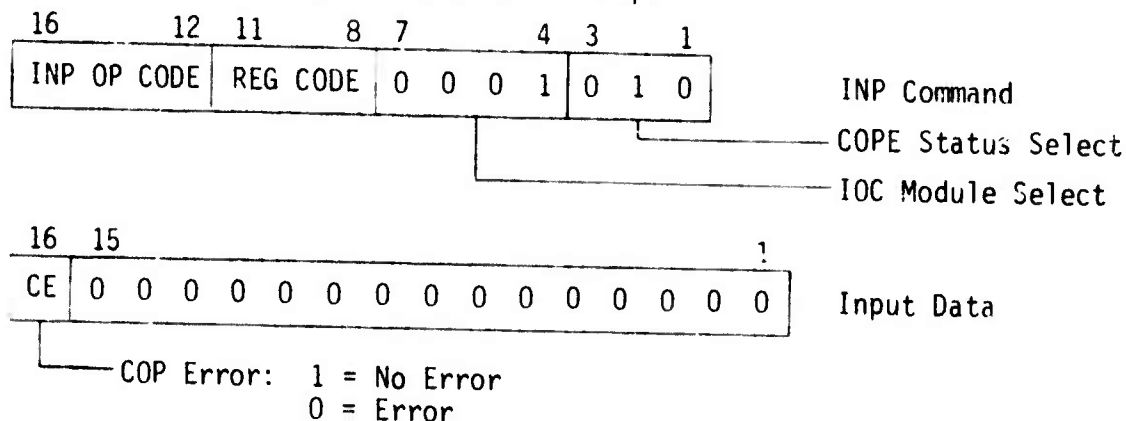
```
 16        12  11       8  7         4  3       1
| OUT OP CODE | REG CODE | 0  0  0  1 | 0  1  0 |   OUT Command
                                          |_____ COPA Designation
                            |_____ IOC Module Select
```

```
 16                                             1
| X  X  X  X  X  X  X  X  X  X  X  X  X  X  X  X |   Output Data
```

```
 16        12  11       8  7         4  3       1
| OUT OP CODE | REG CODE | 0  0  0  1 | 0  1  1 |   OUT Command
                                          |_____ COPB Designation
                            |_____ IOC Module Select
```

```
 16                                             1
| X  X  X  X  X  X  X  X  X  X  X  X  X  X  X  X |   Output Data
```

SECTION IV

PROCESSOR SUPPORT HARDWARE

The support equipment provided with the WCP was a standard Magic 362 Computer Control Console consisting of a paper tape reader and a Computer Control Unit. (See Figure 2.)

The program generates a COP command sequence of COPA, COPB, COPA, COPB, etc. from turn-on. Failure to generate the required sequence results in the setting of a COP Error flag. This flag shall be read witn an INP command which shall not cause an instruction counter skip.

```
 16        12  11      8  7        4  3     1
┌─────────────┬─────────┬─────────┬─────────┐
│ INP OP CODE │ REG CODE│ 0  0  0 1│ 0  1  0 │   INP Command
└─────────────┴─────────┴─────────┴─────────┘
                                    └──── COPE Status Select
                              └────────── IOC Module Select
```

```
 16  15                                        1
┌──┬──────────────────────────────────────────┐
│CE│ 0  0  0  0  0  0  0  0  0  0  0  0  0  0  0│   Input Data
└──┴──────────────────────────────────────────┘
  └── COP Error:  1 = No Error
                  0 = Error
```

Physical Description

The Weapon Control Panel is configured as a single unit measuring approximately 13-1/4 x 8-3/8 x 10-1/4 inches and weighing approximately 35 pounds. The WCP is divided into two primary sections. The front half (Figure 7) contains the display, display electronics, switch matrix, display power supplies, and the I/O circuitry for both the switch matrix and the display. Contained in the rear section (Figure 8) are the Magic 362 computer and external I/O, the computer I/O power supply, interconnect harness and external connectors, and a fan for self-cooling. These elements are identified in Figure 9.

The construction employs a number of features directed toward ease of maintenance which include:

- Connectorized harnessing between the two box halves and from the external connectors to the computer motherboard.

- Completely plug-in electronics.

- Integrated switch matrix, display and switch matrix/display electronics section allowing normal operation with this section removed from the enclosure.

- Connectorized harness from the switch matrix to its electronics.

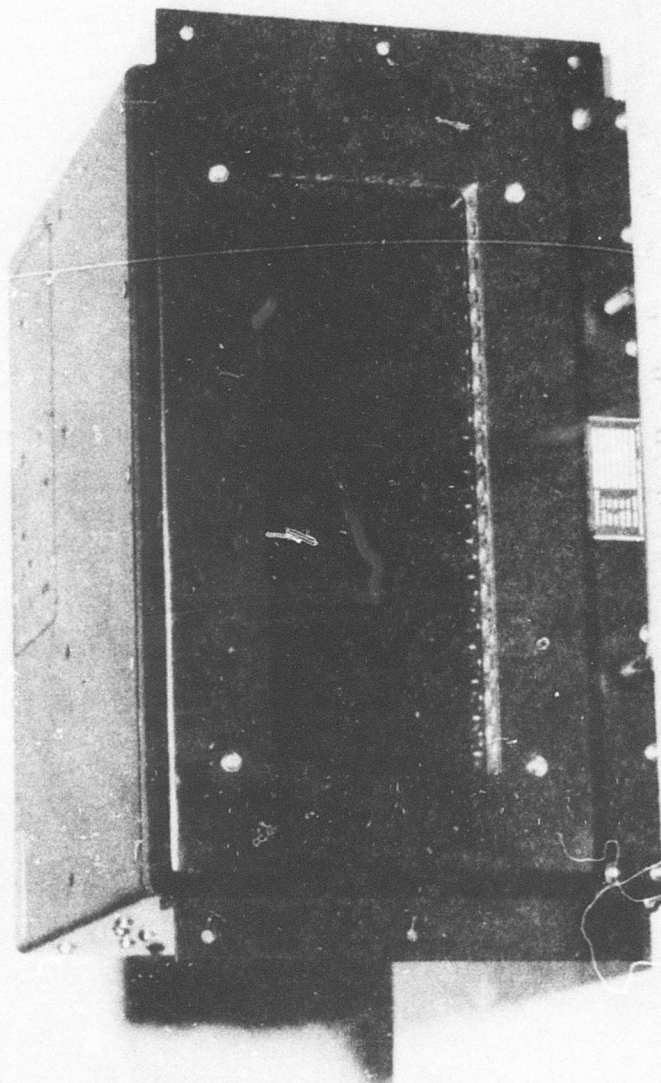- Front panel handle to facilitate installation and removal.

- Self-cooling.
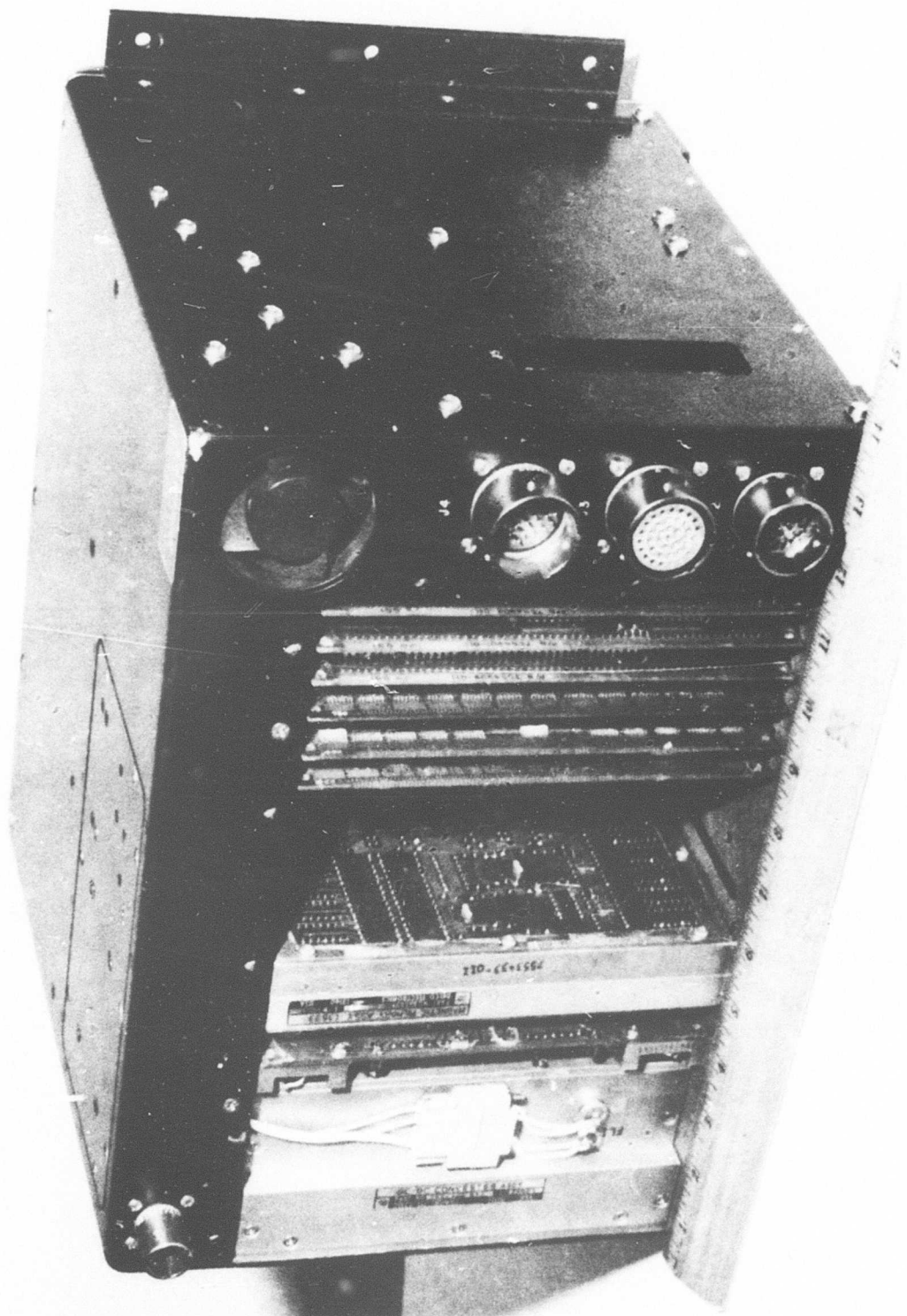
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Figure 7. Weapon Control Panel, Front View

Figure 8. Weapon Control Panel, Rear View

F
G
H
I
J
K
L

M

A-SWITCH MATRIX FRAME
B-SELF-SCAN DISPLAY
C-SELF-SCAN ELECTRONICS CHASSIS
D-M362 POWER SUPPLY
E-COMMON DRIVE ELECTRONICS(Memory)
F-DISCRETE IO MODULE
G-PARALLEL IO MODULE
H-DISPLAY/SWITCH MATRIX INTERFACE MODULE
I-PROCESSOR 2/IO CONTROL MODULE
J-PROCESSOR 1 MODULE
K-MEMORY ELECTRONICS MODULE
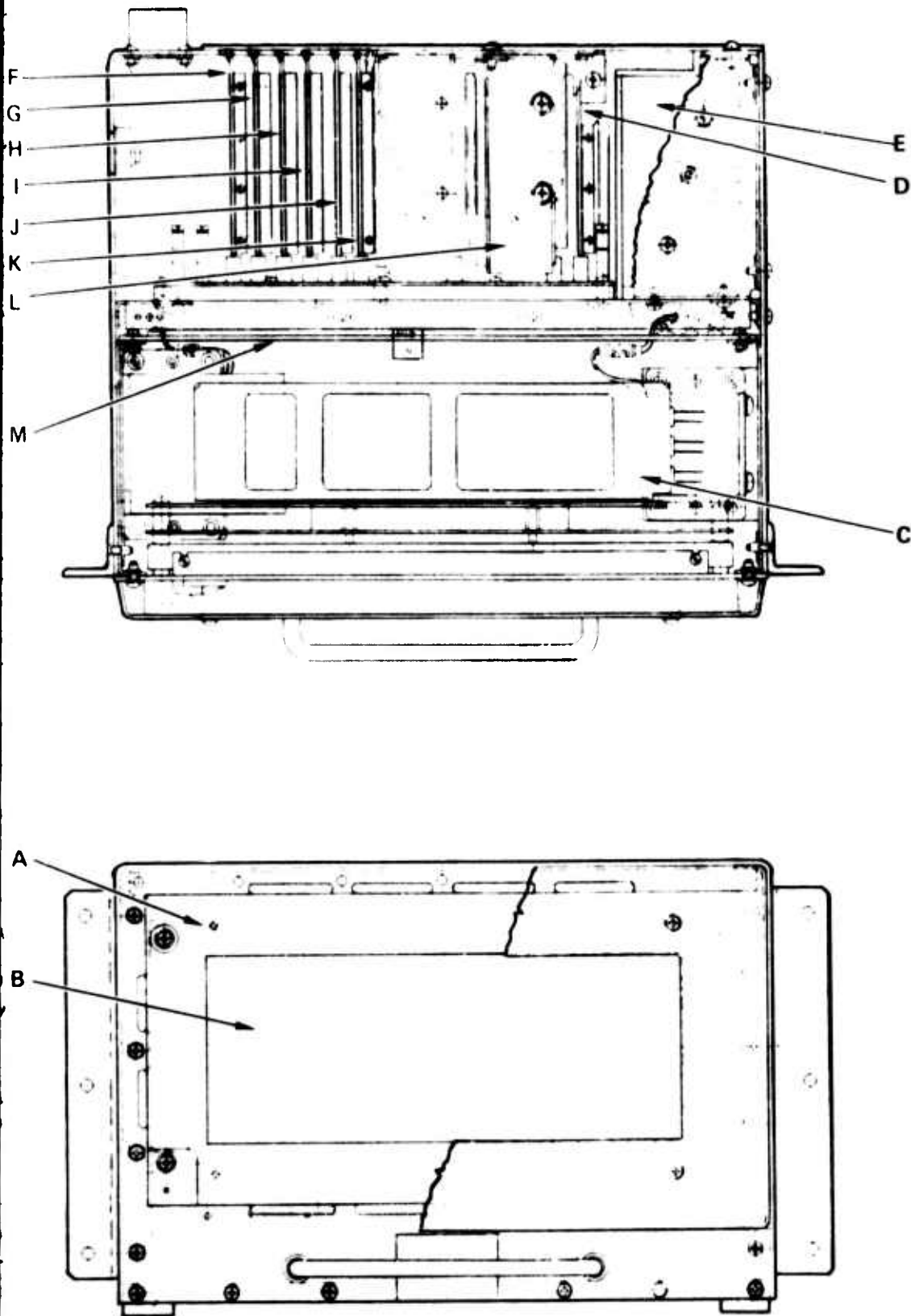L-8K MEMORY MAGNETICS ASSEMBLY
M-DISPLAY/SWITCH ELECTRONICS ASSEMBLY

A

B
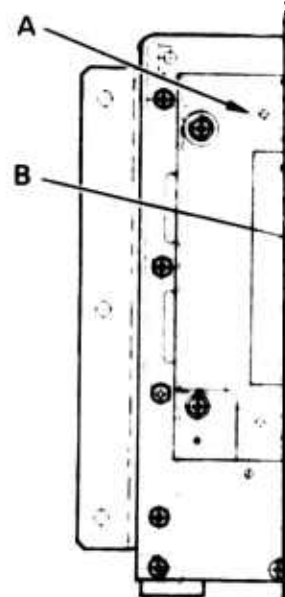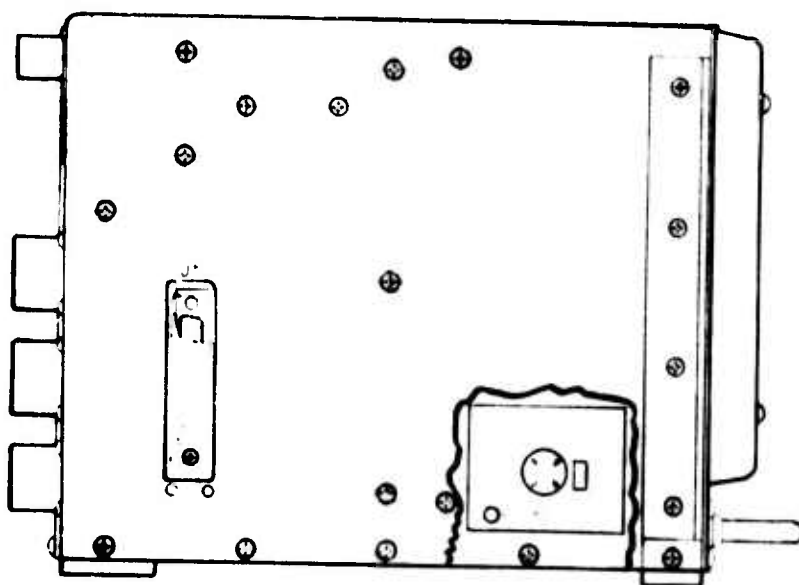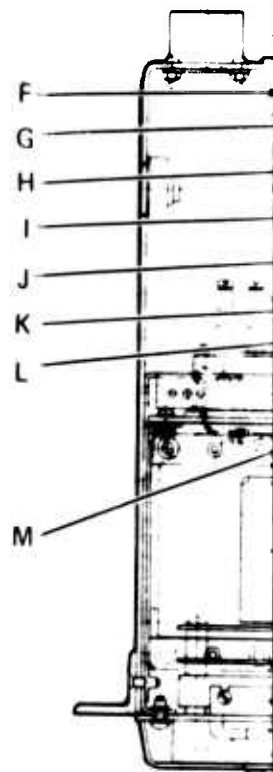
Figure 9. Weapon Control Panel Layout

The Computer Control Unit (CCU) provides control and display capability for all phases of computer operation. It is the main tool in checking the processor and memory and also provides program monitor capability to allow the programmer to monitor, alter, and debug his programs. The CCU functions to:

- Control the compute process.

- Load and read memory and processor registers.

- Respond to input/output instructions.

- Check the interrupt process.

- Display program checkpoints.

- Display processor status.

The CCU consists of a front panel assembly for the controls and displays and one wire-wrapped circuit board containing electronics organized as a processor with central data storage and PROM control memory.

As shown in Figure 10, the Magic 362 tester has four 16-bit octal displays, 52 lights, 39 pushbuttons (including keyboard), 18 switches, and 10 test points. Of the octal displays, one is dedicated to output from M362 (OUTPUT), one is dedicated to input from the keyboard or peripheral (INPUT), and two are selectable. The upper selectable display can read out a M362 register (CREG), the last instruction executed (INST), or the CCU match register (MATCH). The lower selectable display can read out the CCU M362 register address (RAD), the last memory address seen (MA), or the CCU address/instruction register (AD/I). Note that (1) MA and INST may be displayed for checking a sequence of instructions; (2) AD/I and MATCH may be displayed together for keyboard functions and match observations; and (3) CREG, together with the OUTPUT register, can display a 32-bit word for checking double precision.

Operations and Displays

1. Start-up Sequence

The CCU has a power switch, TESTER RESET and COMPUTER RESET pushbuttons, and a CONTROL ENABLE switch. The POWER switch turns on the CCU; it does not apply power to the computer. The TESTER RESET asynchronously sets the PROM address to zero, turns off bus control, and lowers the signal CCC (Computer Control). The COMPUTER RESET switch is a simple pushbutton ground into the computer and does not affect the CCU.

The CCU CONTROL ENABLE switch is normally left on except for system applications. When this switch is off, the CCU becomes only an I/O device and loses its ability to stop the computer or to disable any of the computer's functions. (The CONTROL ENABLE switch overrides the TESTER RESET with respect to the signal CCC.)
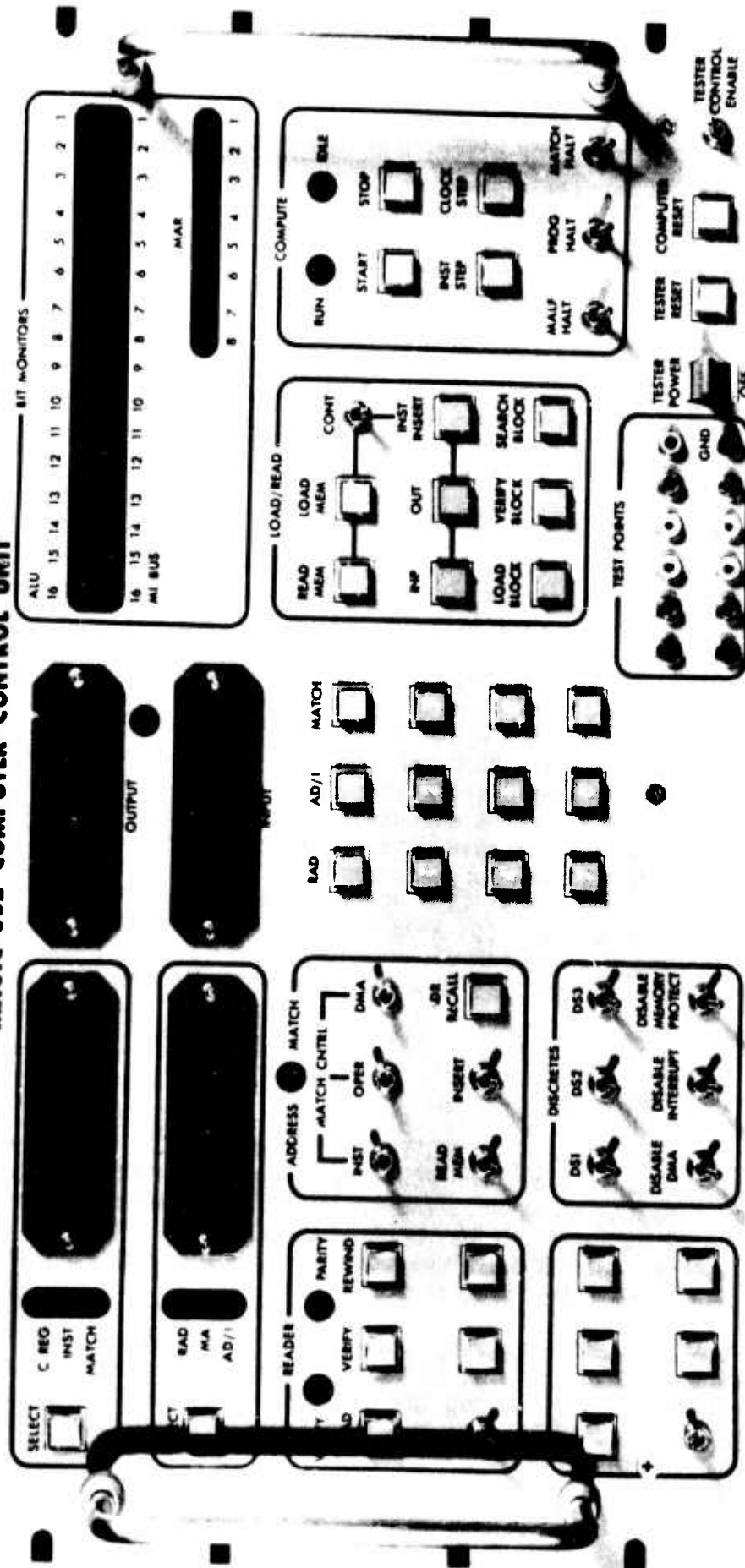
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Figure 10. CCU Front Panel

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2. Selecting the Octal Displays

For the two selectable displays there are indicator lights which show which word is being displayed. Adjacent to each set of lights is a pushbutton. Each time the button is pushed the light will step to the next word.

3. Using the Keyboard

Each time a number is pressed on the keyboard, the number will appear as the right most digit on the INPUT register. All other digits in the INPUT register will shift left at the same time in calculator fashion. The clear (C) button will zero the INPUT register.

After the proper information is entered into the INPUT register, the operator can transfer the information into the address/instruction register (ADI display), the match register (MATCH), or the register address (RAD) register. He can also use the INPUT register as input data to the computer in one of the operations described below.

4. Loading and Reading from Memory

The operator can load or read memory either one location at a time or in blocks. The first is used to check or alter a program and the second is used to verify or debug the memory.

In the single step operation, load data is in the INPUT register, read data is in the OUTPUT register, and the address is in the AD/I register. The AD/I register is automatically incremented by one after each operation. For a load operation, an automatic read operation will follow before the AD/I register is incremented so that the operator can verify the load (i.e., OUTPUT and INPUT displays agree).

The block functions (load, verify, and search) are similar except that the process is automatically repeated until the AD/I equals MATCH. Therefore when a block function is initiated, the start of the block must be in AD/I and the end of the block must be in MATCH. In the search or verify block cases, the process will also stop if the INPUT register equals the OUTPUT (search) or if they are not equal (verify).

Loading or verifying tapes is just a repeating single step operation. The INPUT register is automatically filled from the tape and a read operation will follow a load; that is, verify is automatic when loading. The process stops on a verify error, tape parity error, detected format error, or when no data holes are present (end of tape). When stopping on an error, the AD/I register will not be incremented. This is provided so that when the operator corrects the information manually, the address is already there and, after the manual load, the tape can be restarted from that point.

For interface problems there is a continuous switch which will cause the single step operations to repeat. In this case the AD/I register will remain constant.

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For all of the above, the CCU has the lowest priority in the I/O priority scheme. However, there is a switch on the CCU to disable other I/O devices (DISABLE DMA).

5. Loading and Reading the Registers

The CCU will be able to load and read all 16 of the processor RAM registers. In addition, the microaddress register (MAR) will be displayed continuously on a discrete display.

Loading and reading is done by means cf the instruction insert process. The proper instruction is loaded into the AD/I register by means of the keyboard. Load information is placed in the INPUT register (if loading), and the INSTruction INSERT button is pressed. A read operation will display data in the OUTPUT register.

For the operator, the process is similar to the load/read memory operation except that: (1) the AD/1 register does not increment, and (2) a read operation does not automatically follow a load operation.

For convenience, an automatic insert is provided. This feature inserts one instruction into the M362 every time the M362 is halted. The instruction for this operation is provided by the operator by entering the register address (RAD) register(so named because the selected instruction is almost always used to display an M362 register). When the usual output instruction is inserted, the selected M362 register will appear in the CREG display whenever the computer is halted.

Note that by using both the automatic and manual inserts together, a double precision word can be displayed on the front panel (CREG and OUTPUT displays).

The automatic insert becomes active only after the RAD register has been manually loaded at least once.

6. Input and Output Instructions

The CCU is able to respond to I/O type functions, both for checking this interface and for monitoring test program status or to input program information.

The operator is able to input data words into the program by means of the keyboard and INPUT register or discrete status from switches. He can also observe output data words along with a visual indication that the word has been updated (flashing light).

Because there is a common bus in the M362, it is also possible to simulate input or output instructions. This process is similar to the load/read memory operation, and the simulated instruction is in the AD/I register. The operator simply presses INP to simulate an input instruction and presses OUT to simulate an output instruction. However, one must remember that the INPUT and OUTPUT display registers are labeled from the computer

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standpoint. Therefore, data flows from the INPUT display to the computer I/O when simulating an output instruction, and data flows from the computer I/O to the OUTPUT display when simulating an input instruction.

7. Checking the Interrupt Process

An interrupt in the M362 is an instruction insert, where a transfer instruction is inserted directly into the M362 processor. To perform an interrupt, the desired instruction is entered into the AD/I and the INST INSERT button is pressed.

This process can be made continuous by means of the CONTinuous switch.

8. Controlling the Compute Process

The CCU has START and STOP buttons which control the status of the signal CCC. This signal is displayed as the RUN light. The CCU also has INSTruction STEP and CLOCK STEP buttons. The instruction step works in the usual manner, but since the M362 clock is normally on even when CCC is low (halted), the CLOCK STEP button is somewhat different. The first time the button is depressed, the processor clock will be inhibited. Each time thereafter the processor will execute one microprogram step for each push of the button. The clock will be released again whenever INST STEP, STOP, or START buttons are pressed.

A program may also be halted (1) at a particular memory address, (2) by a program command, or (3) by a malfunction, each by setting the appropriate toggle switch.

9. Displaying Program Checkpoints

The CCU has match capability. A match register, controlled by the operator, is provided and is used to compare to memory addresses. When the match register equals the observed memory address, a visual indication is provided to the operator (flashing light). The operator is able to use the match signal to initiate the read memory or instruction insert process or to halt the computer. Furthermore, the type of memory address used for matching may be controlled with the INSTruction, OPERand, and DMA switches.

Since read memory data and output instruction data both show up in the OUTPUT register, the output instruction display will be inhibited whenever the match DMA switch is used.

The CCU has a minimum recall capability of 16 words. Each time the match ADR RECALL button is pushed, the last address (of the selected type) presented to the memory is displayed in the OUTPUT register until the last 16 have been displayed. When the ADR RECALL button is pushed, the AD/I register will increment. Thus, if the operator zeroes the register prior to using address recall, the AD/I register will indicate which of the 16 words is being displayed.

10. Displaying Processor Status

The CCU has discrete light displays displaying the arithmetic logic unit (ALU), main bus (MI BUS), and the microprogram address register (MAR). For convenience, the idle states of the MAR are decoded and displayed as the IDLE light.

The CCU is also able to monitor one selected register whenever the computer is halted. The register is selected by entering the proper information into the RAD register by means of the keyboard. This is nothing more than an automatic instruction insert, and any type of instruction could be placed in the RAD register if desired.

Test points are provided on the front panel for the following signals:

HLD	$\overline{IOE}$	WR	$\overline{GCIN}$	$\overline{IOR}$
AD		DMA	$\overline{INSR}$	GND
ME		MATCH	CP4	

SECTION V

SOFTWARE

Several software packages were delivered with the equipment to support program
generation of both operational routines and display pages, to support program
checkout and to facilitate WCP testing. Most of the routines provided were
standard Magic 362 software packages with the unique items being the display
page source preparation and linkage to the main program, a switch read and
display unpacking routine and I/O wrap-around test routine.

The software programs operate in a Magic 362 Computer Support Equipment system
comprised of a CAI Alpha-16 minicomputer, a CRT terminal, a dual digital
cassette recorder, a printer, and a M362 controller.

Cross Assembler

The Magic 362/CAI Alpha 16 Cross Assembler assembles and link edits relocat-
able program modules and outputs absolute object data tapes which can be
loaded into the Magic 362 with the Debug program. The program requires 8K
words of memory for the instructions and symbol tables, one or two dual
magnetic tape cassette units, a control console keyboard and CRT, and line
printer. The 8K version uses 4K of memory to provide 750 symbols per module
and 500 external symbols per program. The tables may be easily extended by
adding more memory to the Alpha 16 computer.

The Assembler program consists of a Source Preparation Module for accepting
and editing source data from the keyboard, three Assembler Modules for
processing source data into absolute or relocatable program modules, and
three Linkage Editor modules to assign locations in the Magic 362 and generate
an absolute object tape. The various program modules and a supervisor program
are stored on a single magnetic tape cassette along with the Alpha 16 utility
programs. The system includes an interrupt drive Input/Output Controller to
maximize throughput and provide the user with an easy method of programming
the peripheral I/O devices.

The assembler and linkage editor functions can be operated in an automatic
or manual mode. The system uses a master record concept so that outputs
from any assembler module may be modified by the Source Preparation Module
and used again as source data. The outputs include error and warning
messages, magnetic object data tapes for loading the Magic 362, load maps,
external symbol lists and program listings containing source data object
data and cross reference tables including external symbol addresses.

Display Page Preparation Program

The Display Preparation Program operates in an 8K CAI Alpha 16 computer and
prepares page modules for the Linkage Editor modules in the Magic 362
Assembler. Page modules contain the fixed data to be displayed on the
control panel and provide the program linkages to include variable data within
the fixed data display. The Linkage Editor program combines the instruction
and page modules and the display routines into a single program and generates
an absolute object tape. The Magic 362 Debug Program which operates in the

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Alpha 16 computer loads the object tape into the Magic 362 computer. Figure 11 shows the information flow through the various support programs.

The Display Preparation Program allows the user to prepare a replica of the desired Weapons Control Panel display on the programming console CRT one at a time. The user may indicate variable data and switch points as well as fixed data and may modify the display until the proper format is present on the CRT. When the desired format has been attained, the user directs the program to output the data on magnetic tape. Prior to actually placing the display data for the page on tape, the program requires the user to symbolic-ally define the page and all variables on the page. These same symbols are used to refer to specific displays and variables in the instruction modules of the operating program. The user may read previously prepared page modules from magnetic tape and inspect and correct the old data and output the modified page module on magnetic tape.

The output of this program is a separate module for each display generated. Each module automatically contains the proper NAME statements. Each module prepared by the Display Preparation Program is ready for processing by the LINKAGE EDITOR. The user must insure that the VARIABLE and PAGE NAMES assigned during the WCP ASSIGN NAMES mode are the same as the symbolic names used in the page control programs to reference the display page and its variable areas. Names defined during the WCP ASSIGN NAMES must appear in EXTR statements in the Page Control program where they are to be used.

Magic 362 Operational Routines

The purpose of the operational program for the Weapons Control Panel is to provide control of the Weapons Control Panel through a scenario consisting of display pages each having active switches leading to another page, etc. These two functions are separated into two program sets called MONITOR and SCENARIO, respectively.

The MONITOR routine contains the logic for interpreting switch matrix operation, subroutines for unpacking display data into the virtual display area, controls display blanking for visual feedback during switch operation, and contains subroutines, variable locations and constants common among the page control programs.

The SCENARIO program set consists of pairs of programs, each pair being made up of a Page Control Program and its associated Display Page. The Page Control program provides any initialization required for a particular page, unpacks and moves the DISPLAY PAGE to the virtual area, moves switch trans-fer addresses to the MONITOR switch transfer address table, and may contain logic for servicing its own switches.

Magic 362 Debug Program

The Magic 362 Debug program loads and verifies Magic 362 object tapes, provides inspect and correct capability of the Magic 362 memory and registers in either the idle or run modes, contains block fill and breakpoint directives, and allows the user to start the computer program execution at any location in the run or instruction step mode. The program operates in the CSE Alpha 16 computer and communicates with the user by means of the CRT terminal.
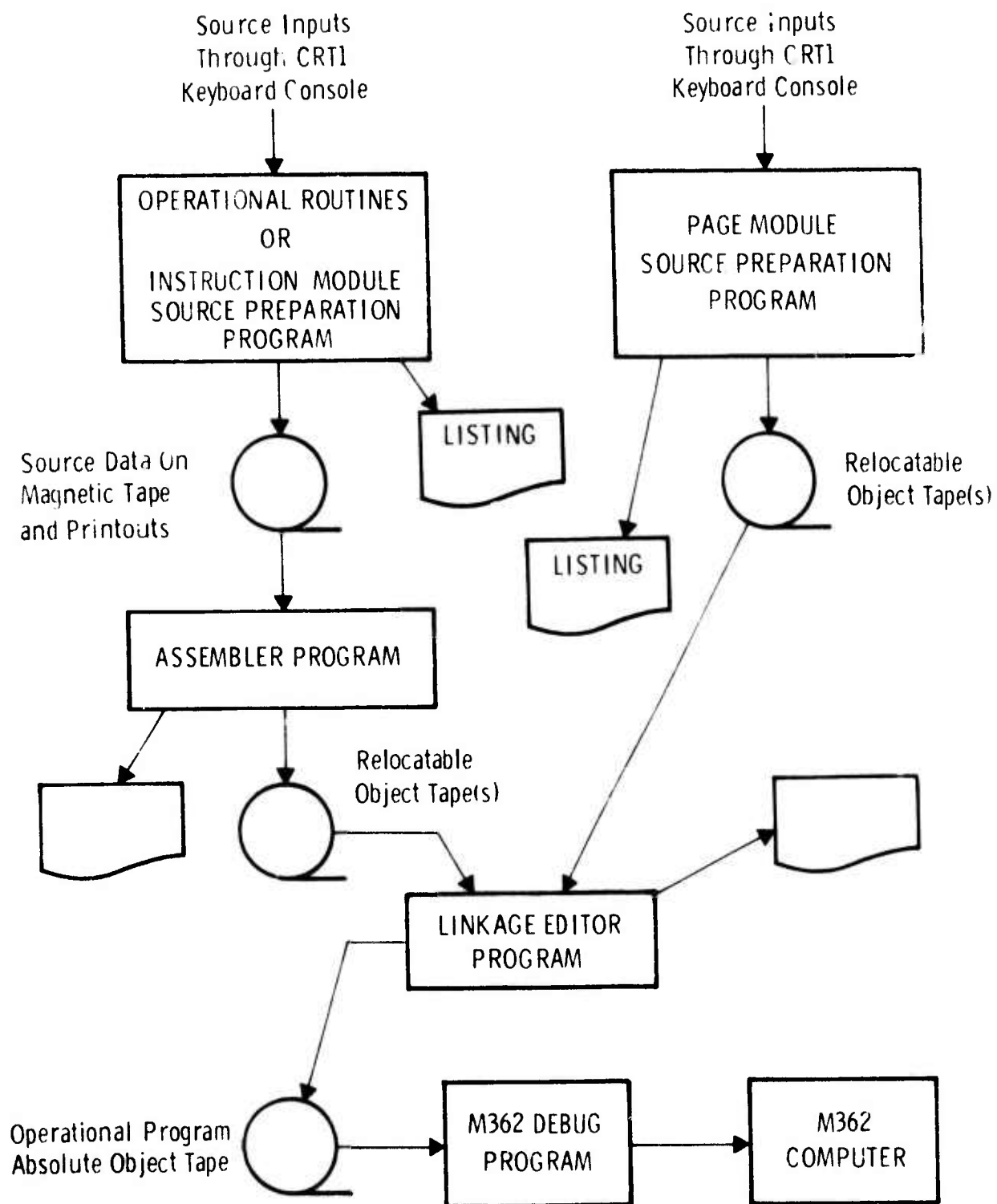
Figure 11. Weapons Control Panel Operational Program Generation

Magic 362 Diagnostic Programs

1. DCS Memory Exerciser Program

The CSE controls the execution of the WCP part of the Memory Exerciser
Program. Program options to select individual memory test patterns are
received by means of the operator typed QTaaa# directive. During execution of
the WCP part of the Memory Exerciser Program, the CSE monitors the cycle
counter and Pass/Fail flags in DCS memory. If a failure is detected, the CSE
halts WCP execution and displays (1) the failed WCP address, (2) the actual
contents of the failed address, and (3) the expected contents of that address.
The CSE then waits for the operator go-ahead.

Initially, the Memory Exerciser program resides in the upper block of WCP
memory, and the lower block of memory is exercised for a specified number
of cycles. Each memory location in that block is loaded and verified to
contain its own address. Then the entire memory block is loaded and verified
with an operator selected pattern. After a pre-selected number of cycles
through memory, the Memory Exerciser Program is moved to the lower block of
memory and the upper block of memory is now exercised as described above. In
order to obtain a rapid store rate, writing into memory is done in blocks of
64 words. Verification is done one word at a time after the entire memory
block has been filled with the test pattern. If an error occurs, the WCP
sets a fail flag for the CSE and waits to continue testing until a go ahead
is received from the CSE. Test patterns are a function of the test directive
and include the following:

Directive	Memory Pattern Tested
QT0#	Cycle all patterns
QT1#	Cycle all zeroes
QT2#	Cycle all ones
QT3#	Cycle alternate ones and zeroes (125252_8)
QT4#	Cycle alternate zeroes and ones (052525_8)
QT5#	Cycle sign bit only (100000_8)
QT6#	Cycle worst case bit pattern
QT7#	Cycle complement of worst case bit pattern

2. Instruction Exerciser Program

The CSE controls execution of the WCP part of the Instruction Exerciser
Program. During execution of the WCP part of the Instruction Exerciser
Program, the CSE monitors the cycle counter and the Pass/Fail flags in WCP
memory. If a failure is detected, a fail message and fail code are displayed
on the CRT and the printer; the CSE then waits for operator go ahead.

The WCP part of the Instruction Exerciser performs the actual testing of each
instruction. Initially, a basic subset of WCP instructions are tested in a
series of computation loops, and checkpoint data is transmitted to the CSE
for validation. After this initial check, this subset of WCP instructions is
used to verify the proper execution of the remaining WCP instructions. If a
failure is detected, a fail flag is set, an error code is transmitted to the
CSE, and the WCP goes into a wait loop until given a go-ahead by the C'E.
During execution of all instruction tests, the test codes are monitored to

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verify that the instruction tests are being performed in the proper order. If not, the fail flag is set. The Instruction Exerciser runs in a continuous loop, repeating the selected instruction tests until execution is terminated by the CSE. Arithmetic operations are generally checked with variable arguments that change with each test iteration.

3. I/O Test Programs

A number of I/O test routines were written to support checkout and troubleshooting of the WCP.

Display Routines - Display diagnostics include four screen patterns to allow determination that all 256 character locations are operative as well as each matrix dot in each character location. Another routine causes the display to be loaded with a page containing all of the 64 possible characters.

Switch Matrix Routines - For switch matrix verification, a routine is provided which displays a locating pattern on the WCP display and portrays the upper-left and lower-right coordinates of an object in the switch matrix field on the CRT terminal. In addition, the status of the switch matrix malfunction discretes is shown on the CRT. By proper placement of an object (finger) in the switch matrix field, proper operation of each X and Y axes switch and the malfunction detection circuitry can be verified. This routine also provides for testing the individual software enable/disable control of X and Y axis switches.

Interrupts - Through the use of an external wrap-around of discretes and parallel channels, interrupt test routines verify the operation and priority level of each interrupt. The control and timing of the real-time interrupt is also tested.

Discretes - The discrete test routine verifies the operation of each input and output discrete using external wrap-around.

Parallel I/O- The parallel I/O routine also uses a wrap-around and external indicators to test each input and output data line as well as the associated control signals.

BITE - The COPE and memory parity error detection circuitry is tested for both normal operation and fault detection.

SECTION VI

RECOMMENDATIONS

During the development of the programmable control and display system and as part of this contract, several tradeoff studies and conceptual analyses were performed to establish a basic configuration. These tradeoffs are summarized at the beginning of Section III. However, since the WCP represents the first system application of the integrated display/switch matrix/processor concept, a number of hardware and application alternatives were only briefly examined and the actual utilization of the hardware has pointed to additional avenues of study and development.

Human Factors Considerations

The man/machine interface between the pilot and the WCP represents a major area of investigation so that the panel can be utilized to the fullest of its capabilities. Primary considerations include organization of the display and optimization of nomenclature, assignment of active switch areas, and switch selection feedback.

1. Display Organization

The display pages typically portray status information (current system mode, previous selections made for multi-page sequences, and relative variable data), option selections associated with the display pages and page change selections such as return to the previous page, return to a master table of contents, and perform self-test. With the flexibility of the panel a conflict arises between the desire to provide the operator with all pertinent data associated with available options and the need to provide a simple, uncluttered display. To achieve a reasonable compromise, studies are required to determine the page organization which provides the highest level of situation comprehension and reaction. Associated with this is the derivation of a set of abbreviations and mnemonics which are easily recognized and understood. The resultant format and nomenclature should be used as standards for all applications.

2. Active Switch Areas

The switch matrix enable/disable software control allows certain areas of the panel to be defined as active switch areas. This function, when used in conjunction with display formatting organization, can be used to minimize ambiguous selections by providing increased physical separation between options. The ability to determine the selected option is further enhanced by providing the processor software with both the upper-left and lower-right coordinates of the object in the switch matrix field. This feature allows a validity check to be made on the object size and further can be used to perform a calculation as to where the operator actually intended to make his selection. Areas open to investigation include the following:

- Determine where operators actually place their finger to make a selection relative to the optimum hardware preferred location, i.e., below and right (probably a right-handed preference), below and left, etc. Also establish the normal area covered by a finger in an

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operational condition (flight gloves plus vibrations). From these factors, software criteria can be established for determination of the actual coordinates as derived from the transferred data. This test would also determine the need for mechanical finger pointing aids such as row separation bars or finger hole overlays to constrain relative motion between the display and the finger.

- Determine where the active switch location should be for each option. While it is desirable to touch the word representing the desired option, the row-to-row spacing (assuming each row is used) may be too close to allow reliable use of full word touch selection. Alternatives to be examined include activation of only the first one, two, or three letters in the word and the use of a staggered listing or the use of a switch designator (such as the symbol*) which would be located alternately in front of and behind the option list words.

3. Switch Selection Feedback

Techniques for providing direct tactile feedback or an audio or visual equivalent should be investigated since the current WCP design provides no physical feel for switch selection. In a demonstration sequence prepared by the contractor, the feedback was provided by blanking all options other than the one selected. Other methods which should be evaluated include:

- An audio click commanded by the processor software when the selection has been recognized.

- A two step selection with the second step showing the selected function with an execute and recall option.

- The addition of a spring-loaded plate over the display where the selection would not be accepted by the processor until the plate was depressed.

Displays

The WCP contains a 256 character alpha-numeric display with approximately 20 fL brightness after the contract enhancement filter. Depending upon the application, different displays and/or increased brightness may be required. Application studies for not only weapon delivery systems but also general avionics control and display requirements should be conducted to determine the most desirable display configuration(s), including the use of fully formatted (graphics) displays. The study should also consider tuning selection capability reqirements (frequency, environmental control, etc.) as well as discrete switch functions.

Software

Part of the page source preparation program and WCP software includes routines for compressing and restoring page data which reduced the average core requirements per page from 128 to 32 words for a typical weapon delivery sequence. Even with this degree of compression, the pyramiding effect of option sequences results in very significant storage requirements. This general

problem should be studied from aspects of:

- More effective compression algorithms.

- Word tables with word selection organized pages rather than the current character-oriented pages.

- Standard pages which are basically common to a number of sequence paths that can be modified with the appropriate unique items by software.

As mentioned previously, various switch selection coordinates determination routines should be evaluated.

Hardware

A number of hardware studies and developments are required before implementing a WCP type system into production aircraft. One of the most significant is the display type and configuration to be used and another is the display technology as determined by function, brightness, and color. In addition, the following should be considered:

- Separation of the display/switch matrix from the processor to reduce depth requirements.

- The design of integrated display and switch matrix logic to minimize circuitry and increase packaging density.

- The design of an integrated panel power supply to increase efficiency and increase packaging density.

- The incorporation of a MIL-STD-1553 data bus into the WCP computer for external interfacing.

INITIAL DISTRIBUTION

Hq USAF (RDQRM)	2	TAWC (TEF)		
Hq USAF (XOXFCM)	1	AFATL (DL)		
Hq USAF (XOOW)	1	AFATL (DLXP)		
Hq USAF (SAMID)	1	AFATL (DLOSL)	2	
Hq USAF (SAMI)	1	AFATL (DLMP)	1	
ASD (ENYS)	1	AFATL (DLMB)	1	
ASD (ENYEHM)	1	AFATL (DLJK)		
FTD (PDXA)	1	AFATL (DLM)	1	
TAC (DRAR)	1	AFATL (DLY)	2	
TAC (LGWM)	1	AFATL (DLJC)	1	
SAC (LGW)	1			
WRAMA (MMEBL)	1			
AFWL (SUL)	1			
AUL (AUL/LSE-70-239)	1			
57 FWW (DOTH)	1			
USAFTFWC (DR)	1			
Redstone Sci Info Ctr	2			
Hq USA Training & Doctrine Comd (ATCD-CS-F-AT)	1			
USN Weapon Lab (Code MIL)	1			
Naval Ordnance Stn (Tech Lib)	1			
USN Ord Lab (Code 730)	2			
USNWC (Code 753)	1			
Nav Wpns Eval Fac (Code W)	1			
Naval Research Lab (Code 2627)	1			
USN Research Lab (Code 7780)	1			
Sandia Laboratories	1			
The Rand Corporation	1			
DDC	2			
AFAL (AAD-1)	1			
AFFDL (FGR)	1			
AEDC (ARO, Inc)	1			
Harry Diamond Lab (AMXDO-DA)	1			
ASD (ENVW)	1			
USA Aviation School (ATSAV-CTD)	1			
Dept of Navy, Power Prog Ofc 473	1			
USNWC (Code 5054)	1			
Ofc of Ch Naval Op (OP-982E)	1			
AFAL (TEO)	1			
AFWL (SECA)	1			
Ogden ALC (MMNOP)	2			
AFWL (LR)	2			
AFIS (INTA)	1			
ADTC (XRC)	1			
TAWC (TRADOCLO)	1			
TAWC (TEFA)	1			
TAWC (TER)	1			